Preliminary Specification

RCL Semiconductors Ltd.

Quadruple Bus Buffers With 3-State Outputs HC125

GENERAL DESCRIPTION

HC125 is fabricated in the high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

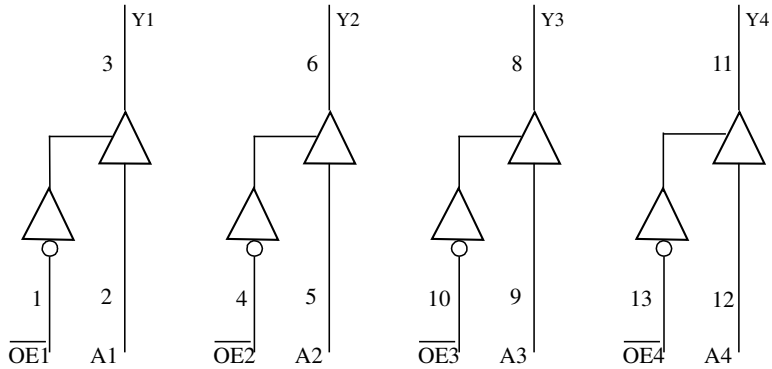
These quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable input ($\overline{OE}$) is high.

$\overline{OE}$ should be tied to VDD through a pull-up resistor to ensure the high-impedance state during power up or power down; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FEATURES

- Wide operating supply voltage range: 2 - 6V
- Output Drive at VDD = 5V : ±6mA
- Typical propagation delay: 11ns
- Low input current: < 1μA.
- Low quiescent supply current: 80μA maximum
- High-Current 3-state outputs interface directly with system Bus

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Truth Table

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)
Z = high impedance state

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (V_{DD})	- 0.5 ~ + 7.0	V
DC input or output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{DD} +0.5	V
DC output Current, any output (I_{out})	±35	mA
DC Current through V_{DD} or GND (Icc)	±70	mA
Storage Temperature(T_{STG})	-65 ~ +150	^{o}C

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Normal	Max.	Unit
DC Supply Voltage (VDD)		2.0	5.0	6.0	V
VIH High-level Input Voltage	VDD=2.0V VDD=4.5V VDD=6.0V	1.5 3.15 4.2			V
VIL Low-level Input Voltage	VDD=2.0V VDD=4.5V VDD=6.0V			0.5 1.35 1.8	V
VI Input Voltage		0		VDD	V
VO Output Voltage		0		VDD	V
Operating Temperature (TA)	74HC125	-40		+85	^{o}C
	54HC125	-55		+125	^{o}C
Input Rise/Fall Times (tr, tf)	VDD=2.0V VDD=4.5V VDD=6.0V			1000 500 400	ns

Note: 2. All unused inputs of the device must be held at VDD or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

(unless otherwise specified)

Parameter	Test Conditions		VDD	TA =25 ^{o}C			54HC125		74HC125		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
VOH	VI=VIH or VIL	IOH = -20μA	2.0V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6.0V	5.9	5.999		5.9		5.9		
		IOH = -6mA	4.5V	3.98	4.3		3.7		3.84		
		IOH = -7.8mA	6.0V	5.48	5.8		5.2		5.34		
VOL	VI=VIH or VIL	IOL = 20μA	2.0V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6.0V		0.001	0.1		0.1		0.1	
		IOL = 6mA	4.5V		0.17	0.26		0.4		0.33	
		IOL = 7.8mA	6.0V		0.15	0.26		0.4		0.33	
I_I	VI=VDD or 0		6.0V		±0.1	±100		±1000		±1000	nA
IOZ	VO =VDD or 0		6.0V		±0.01	±0.5		±10		±5	μA
Icc	VI=VDD or 0	IO =0	6.0V			8		160		80	μA
Ci			2~6V		3	10		10		10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF)

Parameter	From (Input)	To (Output)	VDD	TA =25 °C			54HC125		74HC125		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
t_{pd}	A	Y	2.0V		48	120		150		150	ns
			4.5V		14	24		36		30	
			6.0V		11	20		25		26	
t_{en}	$\overline{OE}$	Y	2.0V		53	120		180		150	ns
			4.5V		14	24		36		30	
			6.0V		11	20		31		26	
t_{dis}	$\overline{OE}$	Y	2.0V		30	120		180		150	ns
			4.5V		15	24		36		30	
			6.0V		14	20		31		26	
t_t		Any	2.0V		28	60		90		75	ns
			4.5V		8	12		18		15	
			6.0V		6	10		15		13	

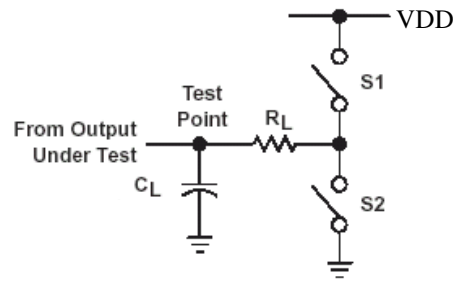
AC ELECTRICAL CHARACTERISTICS (C_L = 150pF)

Parameter	From (Input)	To (Output)	VDD	TA =25 °C			54HC125		74HC125		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
t_{pd}	A	Y	2.0V		67	150		225		190	ns
			4.5V		19	30		45		38	
			6.0V		15	25		39		32	
t_{en}	$\overline{OE}$	Y	2.0V		100	135		200		170	ns
			4.5V		20	27		40		34	
			6.0V		17	23		34		29	
t_t		Any Q	2.0V		45	210		315		265	ns
			4.5V		17	42		63		53	
			6.0V		13	36		53		45	

Parameter	Test Conditions	Typ.	Unit
C_{pd} Power Dissipation Capacitance	TA =25 °C , No Load	45	pF

Note 3: C_{PD} determines the no load dynamic power consumption , $P_D=C_{PD} \cdot VDD^2 \cdot f + Icc \cdot VDD$, and the no load dynamic current consumption, $Is = C_{PD} \cdot VDD \cdot f_i + Icc$

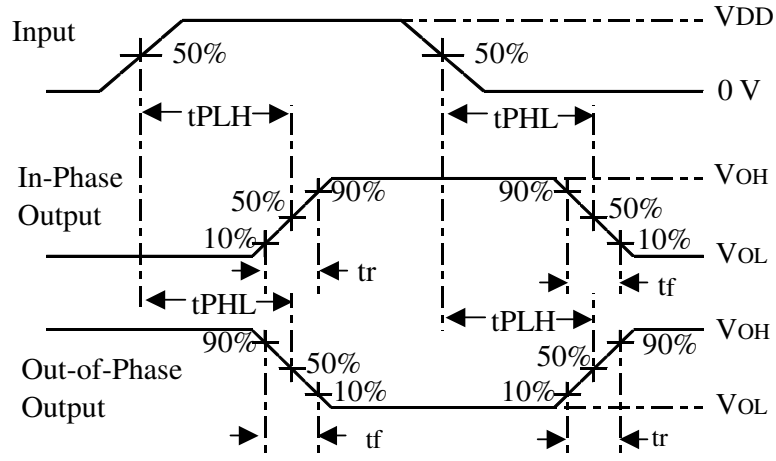
AC TEST CIRCUIT AND AC SWITCHING WAVEFORM



PARAMETER		R_L	C_L	S1	S2
ten	t_{PZH}	1kΩ	50pF or 150pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1kΩ	50pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		---	50pF or 150pF	Open	Open

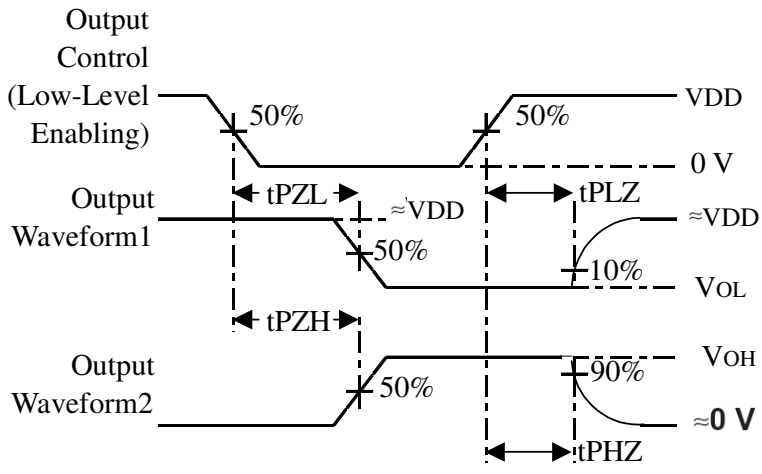
Voltage Waveforms

Input Rise and Fall Times



Voltage Waveforms

Propagation Delay and Output Transition Times



Voltage Waveforms

Enable and disable times for 3-state outputs

NOTES 4: 1) C_L includes probe and test-fixture capacitance.

2) Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3) Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:
PRR ≤1 MHz, Z_O = 50 ., tr = 6 ns, tf = 6 ns.

4) The outputs are measured one at a time with one input transition per measurement.

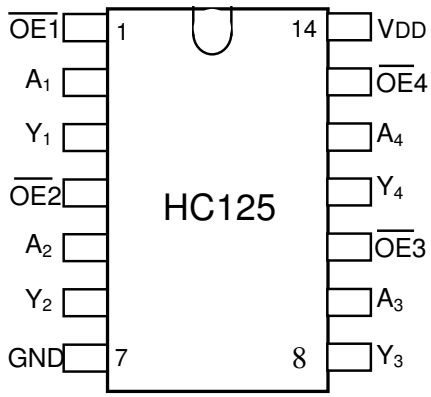
5) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

6) t_{PZL} and t_{PZH} are the same as t_{en}.

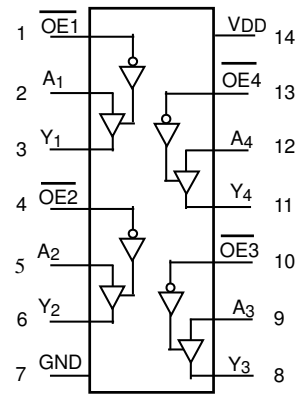
7) t_{PLH} and t_{PHL} are the same as t_{pd}.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
2, 5, 9, 12	A1, A2, A3, A4	Data Inputs
3, 6, 8, 11	Y1, Y2, Y3, Y4	Outputs
7	GND	Ground (0V)
1, 4, 10, 13	$\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$, $\overline{OE4}$	Associated output-enable
14	VDD	Positive power supply

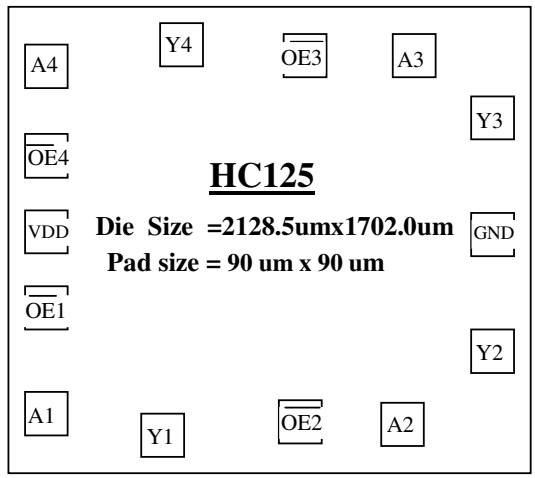


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

A1 (-491.7, -411.4)	A3 (234.9, 321.6)
Y1 (-189.3, -430.7)	$\overline{OE3}$ (31.7, 321.6)
$\overline{OE2}$ (31.7, -411.4)	Y4 (-189.3, 340.9)
A2 (234.9, -411.4)	A4 (-491.7, 321.6)
Y2 (401.7, -265.9)	$\overline{OE4}$ (-491.7, 118.4)
GND (401.7, - 44.9)	VDD (-491.7, -44.9)
Y3 (401.7, 176.1)	$\overline{OE1}$ (-491.7, -208.2)

Note: Substrate should be connected to VDD or left it open.

PAD IDENTIFICATION