RCL Semiconductors Ltd.

3-Line to 8-Line Decoders HC138

GENERAL DESCRIPTION

HC138 is fabricated in the high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

HC138 devices can be used in high-performance memory-decoding or data routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than typical access time of the memory. This means the effective system delay introduced by the decoders is negligible.

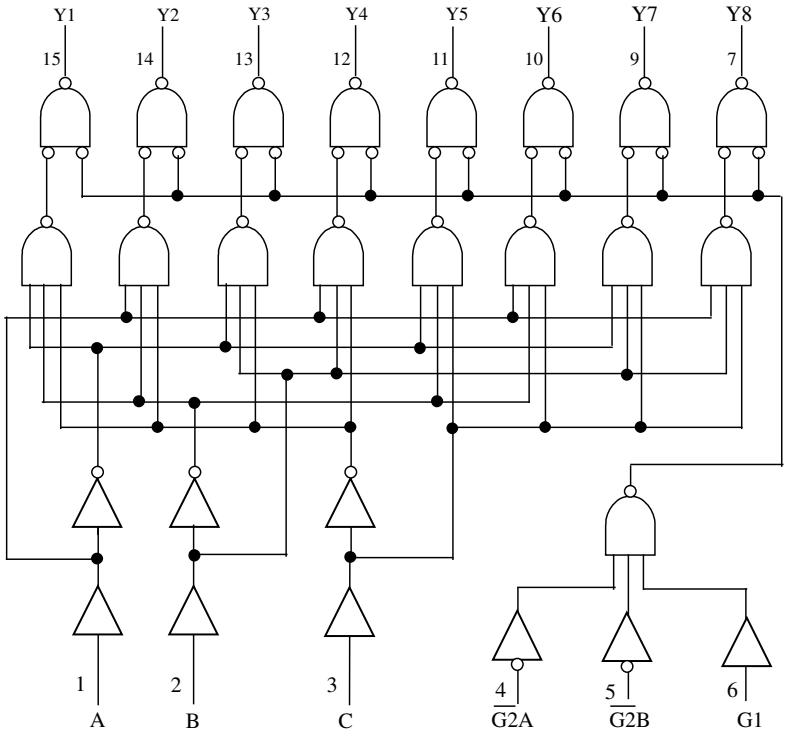
HC138 has 3 binary-select inputs (A, B, C). If the device is enable, these inputs determine which one of the eight outputs normally at high will go low. Two active low and one active high enables (G1, $\overline{G2}$A, $\overline{G2}$B) are provided to ease the cascading of decoders.

A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for de-multiplexing applications.

FEATURES

- Wide operating supply voltage range: 2-6V
- Output Drive at V_{DD} = 5V : ±4mA
- Typical propagation delay: 15ns
- Low input current: < 1μA.
- Low quiescent supply current: 80μA maximum
- Incorporate 3 enable inputs to simplify cascading and/or data reception
- For high-speed memory decoders and data-transmission systems

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2}$A	$\overline{G2}$B	C	B	A	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (V_{DD})	- 0.5 ~ + 7.0	V
DC input or output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{DD} +0.5	V
DC Current Drain per pin, any output (I_{out})	±25	mA
DC Current Drain per pin, V_{DD} or GND (Icc)	±50	mA
Storage Temperature(T_{STG})	-65 ~ +150	^{o}C

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Normal	Max.	Unit
DC Supply Voltage (V_{DD})		2.0	5.0	6.0	V
V_{IH} High-level Input Voltage	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V	1.5 3.15 4.2			V
V_{IL} Low-level Input Voltage	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V			0.5 1.35 1.8	V
V_I Input Voltage		0		V_{DD}	V
V_O Output Voltage		0		V_{DD}	V
Operating Temperature (TA)	74HC138	-40		+85	^{o}C
	54HC138	-55		+125	^{o}C
Input Rise/Fall Times (tr, tf)	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V			1000 500 400	ns

Note: 2. All unused inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

(unless otherwise specified)

Parameter	Test Conditions		VDD	TA =25 °C			54HC138		74HC138		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	V_I=V_{IH} or V_{IL}	I_{OH} = -20μA	2.0V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6.0V	5.9	5.999		5.9		5.9		
		I_{OH} = -4mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH} = -5.2mA	6.0V	5.48	5.8		5.2		5.34		
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} = 20μA	2.0V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6.0V		0.001	0.1		0.1		0.1	
		I_{OL} = 4mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2mA	6.0V		0.15	0.26		0.4		0.33	
I_I	V_I=V_{DD} or 0		6.0V		±0.1	±100		±1000		±1000	nA
Icc	V_I=V_{DD} or 0	I_O =0	6.0V			8		160		80	μA
Ci			2~6V		3	10		10		10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF)

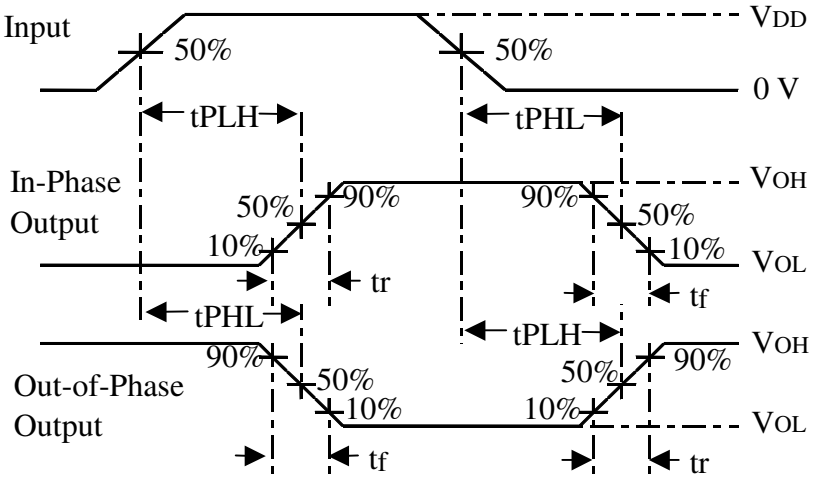
Parameter	From (Input)	To (Output)	VDD	TA =25 °C			54HC138		74HC138		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
t_{pd}	A,B or C	Any Y	2.0V		67	180		270		225	ns
			4.5V		18	36		54		45	
			6.0V		15	31		46		38	
	Enable	Any Y	2.0V		66	155		235		195	ns
			4.5V		18	31		47		39	
			6.0V		15	26		40		33	
t_t		Any	2.0V		38	75		110		95	ns
			4.5V		8	15		22		19	
			6.0V		6	13		19		16	

Parameter	Test Conditions	Typ.	Unit
C_{pd} Power Dissipation Capacitance	TA =25 °C , No Load	85	pF

Note 3: C_{PD} determines the no load dynamic power consumption , $P_D=C_{PD}\cdot V_{DD}^2\cdot f + Icc \cdot V_{DD}$, and the no load dynamic current consumption, $Is = C_{PD}\cdot V_{DD}\cdot f_i + Icc$

AC SWITCHING WAVEFORM

Voltage Waveforms
Input Rise and Fall Times

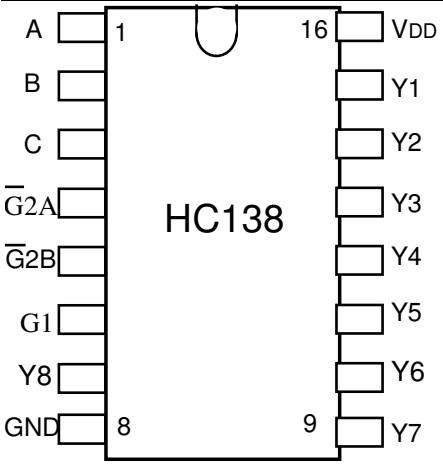


Voltage Waveforms
Propagation Delay and Output Transition Times

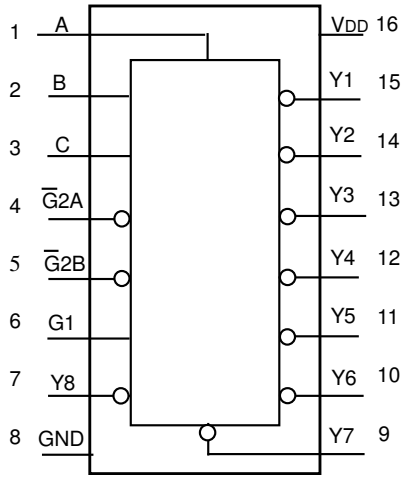
NOTES 4:
1) C_L includes probe and test-fixture capacitance.
2) Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:
PRR $\leq$1 MHz, $Z_O = 50\Omega$., tr = 6 ns, tf = 6 ns.
3) The outputs are measured one at a time with one input transition per measurement.
4) t_{PLH} and t_{PHL} are the same as tpd.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1, 2, 3	A, B, C	Data Select Inputs
15 - 9, 7	Y1-Y8	Data Outputs
8	GND	Ground (0V)
4, 5, 6	$\overline{G}$2A, $\overline{G}$2B, G1	Enable Inputs
16	V_{DD}	Positive power supply

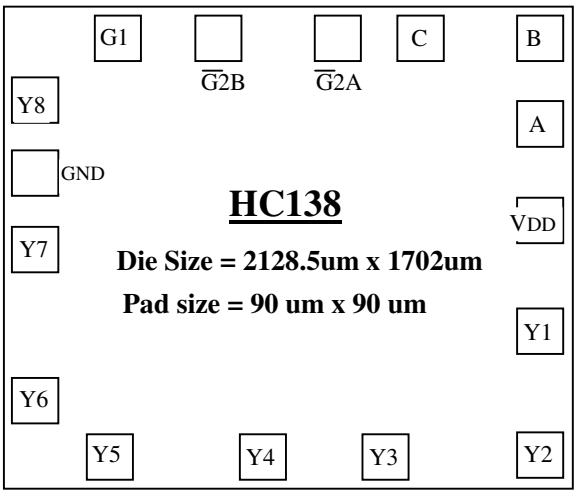


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

A	(429.4, 178.2)	Y7	(-519.3, -57.4)
B	(429.4, 337.7)	Y6	(-519.3, -342.8)
C	(206.4, 337.7)	Y5	(-381.2, -446.8)
$\overline{G}$2A	(48.2, 337.7)	Y4	(- 92.1, -446.8)
$\overline{G}$2B	(-174.8, 337.7)	Y3	(139.9, -446.8)
G1	(-365.3, 337.7)	Y2	(428.7, -446.8)
Y8	(-519.3, 222.8)	Y1	(429.4, -210.4)
GND	(-519.3, 82.7)	VDD	(429.4, - 3.3)

Note: Substrate should be connected to VDD or left it open.

PAD IDENTIFICATION