Preliminary Specification

RCL Semiconductors Ltd.

HEX Schmitt-trigger Inverters HC14

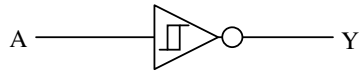
GENERAL DESCRIPTION

The HC14 contains six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

FEATURES

- Typical propagation delay: 11ns
- Wide operating supply voltage range: 2-6V.
- Low Power Consumption, 20-μA Max Icc.
- Low input current: < 1μA.
- Fanout of 10 LS-TTL Loads
- Output Drive at 5 V : ±4-mA

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

1. Truth Table

INPUT A	OUTPUT Y
H	L
L	H

H = High Level (steady state). L= Low Level (steady state)

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Supply voltage (VDD)	- 0.5 ~ + 7.0	V
Input clamp current , I_{IK} (V1 < 0 or V1> VDD)	±20	mA
Output clamp current , I_{OK} (V0 < 0 or V0> VDD)	±20	mA
Continuous output current , Io (Vo = 0 to VDD)	±25	mA
Continuous current through VDD or GND	±50	mA
Storage temperature range , T_{stg}	-65 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

2.The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITONS

Parameter		Min.	Normal	Max.	Unit
DC Supply Voltage (VDD)		2	5	6	V
V_I Input Voltage		0		VDD	V
V_O Output Voltage		0		VDD	V
T_A Operating temperature	54HC14	-55		125	℃
	74HC14	-40		85	

Note: 3. All unused inputs of the device must be held at VDD or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

(T_A=25℃)

Parameter	Symbol	Typ.	Unit	Guaranteed Limit		VDD	Test Condition	
				Min	Max			
Maximum Positive going Threshold Voltage	V_{T+}	1.2 2.5 3.3	V	0.7 1.55 2.1	1.5 3.15 4.2	2V 4.5V 6V		
Minimum Negative going Threshold Voltage	V_{T-}	0.6 1.6 2	V	0.3 0.9 1.2	1 2.45 3.2	2V 4.5V 6V		
Maximum Positive going- Minimum Negative Threshold Voltage	VT+ -VT-	0.6 0.9 1.3	V	0.2 0.4 0.5	1.2 2.1 2.5	2V 4.5V 6V		
Minimum High Level Output Voltage	V_{OH}	VDD-0.002 VDD-0.001	V	VDD-0.1		2V 4.5-6V	I_{OH}= -20μA	V_I=V_{IH} or V_{IL}
		4.3		3.98 3.7 3.84		4.5V	I_{OH} =- 4mA (54HC) (74HC)	
		5.8		5.48 5.2 5.34		6V	I_{OH} = -5.2mA (54HC) (74HC)	
Maximum Low Level Output Voltage	V_{OL}	0.002 0.001	V		0.1 0.1	2V 4.5-6V	I_{OL} = 20μA	V_I=V_{IH} or V_{IL}
		0.17			0.26 0.4 0.33		I_{OL} = 4mA (54HC) (74HC)	
		0.15			0.26 0.4 0.33		I_{OL} = 5.2mA (54HC) (74HC)	
Maximum Input Current	I_I	±1.0	nA		±100 ±1000	6V	(54HC or 74HC)	Vin = VDD or GND
Maximum Supply Current	Icc	-	μA		2 40 20		 (54HC) (74HC)	Vin =VDD or Iout = 0
	Ci	3	pF		10	2-6V		
Power dissipation capacitance per inverter	Cpd	20	pF				No load	

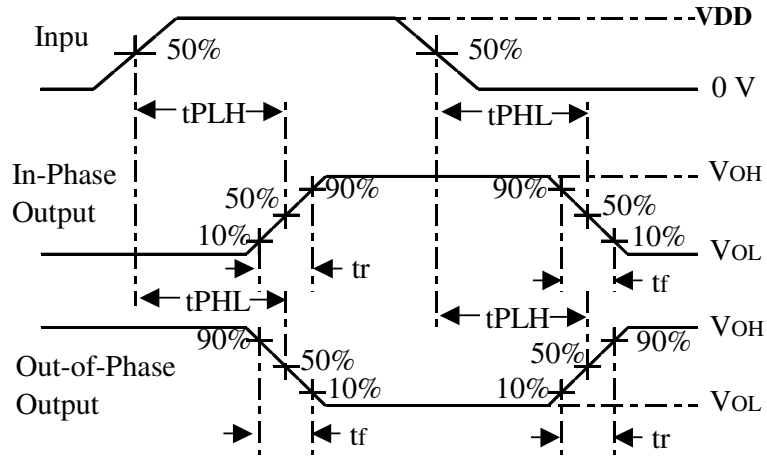
AC ELECTRICAL CHARACTERISTICS

(T_A=25℃ , C_L = 50pF)

Parameter	Symbol	INPUT	OUTPUT	VDD	Typ.	Unit	Guaranteed Limit	54HC	74HC
Maximum Power Dissipation	t_{pd}	A	Y	2V	55	ns	125	190	155
				4.5V	12		25	38	31
				6V	11		21	32	26
transit time	t_t		Y	2V	38	ns	75	110	95
				4.5V	8		15	22	19
				6V	6		13	19	16

AC SWITCHING WAVEFORM AND AC TEST CIRCUIT

VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

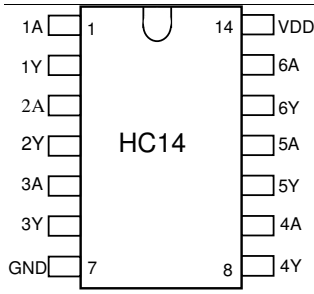


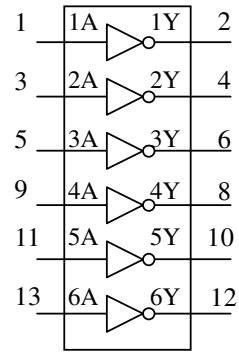
INPUT RISE AND FALL TIMES

Note : 4.CL include probe and test-fixture capacitance.
5.Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics : PRR≤1MHz, Zo=50Ω, tr =tf= 6ns.
6.The outputs are measured one at a time with one input transition per measurement.
7.tPLH and tPHL are the same as tpd.

PIN DESCRIPTION

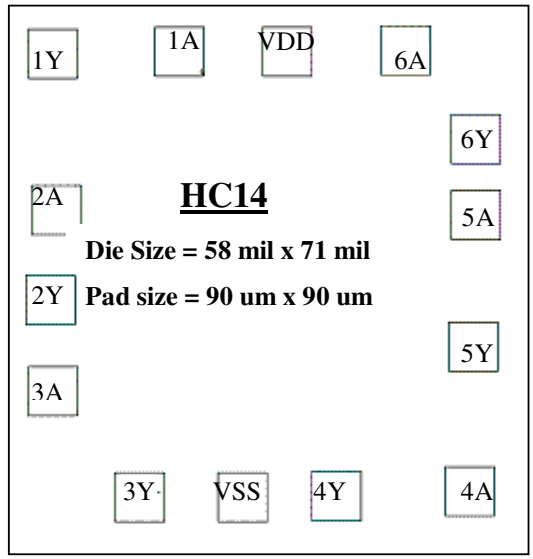
PIN NO.	SYMBOL	DESCRIPTION
1, 3 ,5 ,9 ,11 , 13	1A-6A	Data Inputs
2, 4 ,6 ,8 ,10 , 12	1Y-6Y	Outputs
7	GND	Ground (0V)
14	VDD	Positive power supply





Pin Configuration Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

3Y	(-369.2, -547.3)	6A	(282.2, 457.3)
VSS	(-143.5, -547.3)	VDD	(66.5, 457.3)
4Y	(56.9, -547.3)	1A	(-148.5, 457.3)
4A	(410.7, -547.3)	1Y	(-508.1, 457.3)
5Y	(429.1, - 376.9)	2A	(-519.0, 241.8)
5A	(429.0, -48.5)	2Y	(-519.0, -86.7)
6Y	(429.0, 145.2)	3A	(-519.0, -275.4)

Note: Substrate should be connected to VDD or left it open.