# RCL Semiconductors Ltd.

## 8-Bit Parallel-Load Shift Register HC165

### GENERAL DESCRIPTION

The HC165 is fabricated with high speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

This 8-bit Shift Register has gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the another input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only Data meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8- bit Register during the positive edge of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear (CL) input.

The HC165 logic is functionally as well as pin-out compatible with the standard LS164. All inputs are protected from ESD damage by internal diode clamps to VDD and ground.

Clocking is accomplished by a low-to-high transition of the clock (CK) input while SH/$\overline{LD}$ is held high and CK INH is held low. The functions of CK and CK INH are interchangeable. Since a low CLK and a low-to-high transition of CK INH also accomplish clocking, CK INH should be changed to the high level only while CK is high. Parallel loading is inhibited when SH/LD is held high. While SH/LD is low, the parallel inputs to the register are enabled independently of the levels of the CK, CK INH, or serial (SER) inputs.

### FEATURES

- Typical propagation delay: 13ns
- Wide operating supply voltage range: 2-6V.
- Low input current: < 1μA.
- Low quiescent supply current: 80μA maximum (74HC series).
- Outputs Can Drive Up To 10 LSTTL Loads
- ±4-mA Output Drive at 5 V
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

### FUNCTIONAL DESCRIPTION

**1. Truth Table**

| Inputs | | | Function |
|---|---|---|---|
| SH/$\overline{LD}$ | CK | CK INH | |
| L | X | X | Parallel load |
| H | H | X | No change |
| H | X | H | No change |
| H | L | ↑ | Shift |
| H | ↑ | L | Shift |

H = High Level (steady state). L= Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Note: Shift is the content of each internal register shifts toward serial output QH. Data at SER is shifted into the first register.

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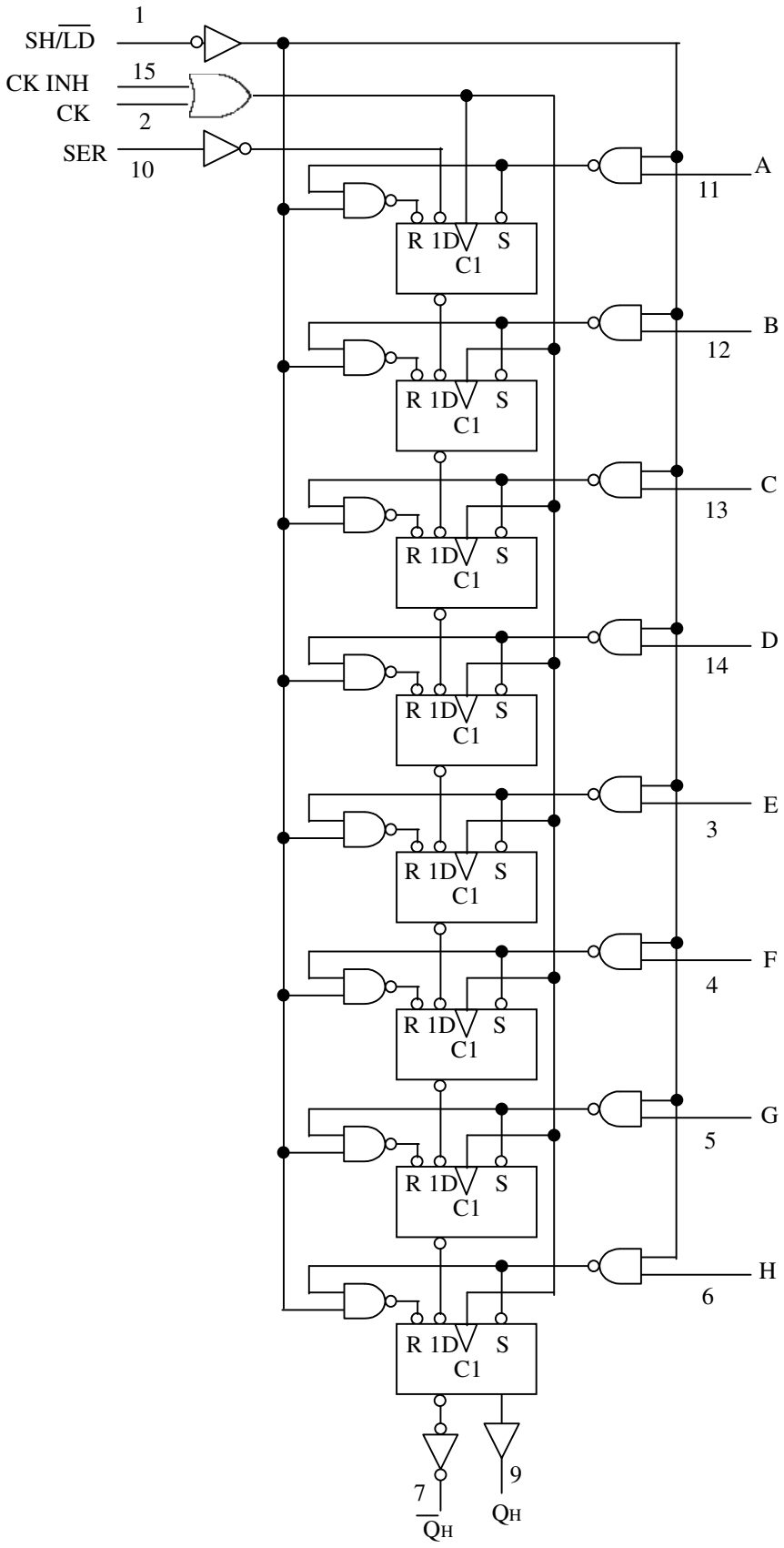
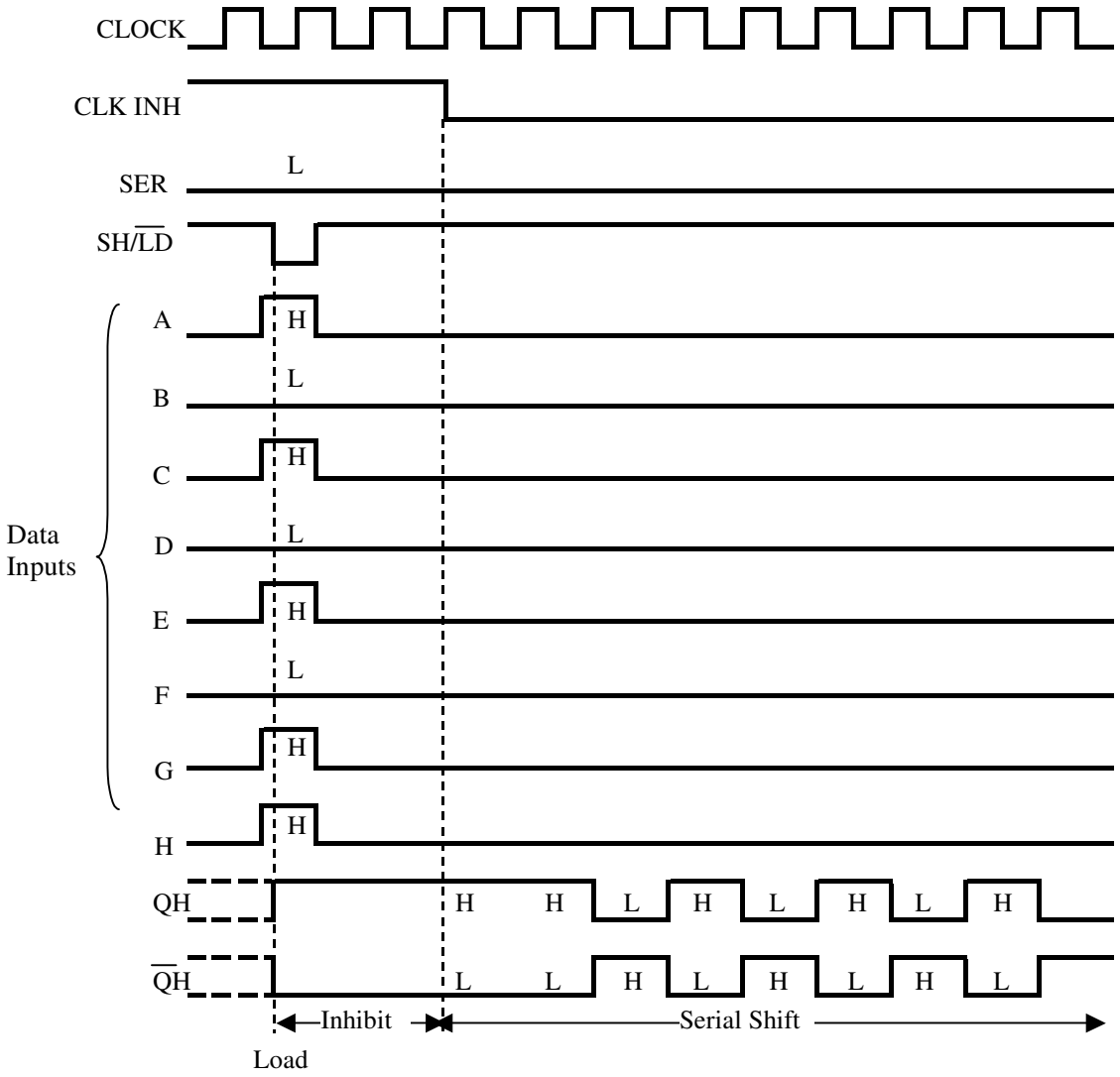
**LOGIC DIAGRAM**



**2. Logic Waveform**




**ABSOLUTE MAXIMUM RATINGS**

| Parameter | Value | Unit |
|---|---|---|
| DC supply voltage (VDD) | - 0.5 ~ + 7.0 | V |
| DC input or output Voltage ($V_{IN}$, $V_{OUT}$) | -0.5 to VDD +0.5 | V |
| DC Current Drain per pin, any output ($I_{out}$) | ±20 | mA |
| DC Current Drain per pin, VDD or VSS (Icc) | ±50 | mA |
| Storage Temperature( $T_{STG}$) | -65 ~ +150 | ℃ |
| Power Dissipation ($P_D$ ) | 500 | mW |
| Lead Temperature($T_L$) (Soldering, 10seconds) | 300 | ℃ |

**Note:** 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter | | Min. | Normal | Max. | Unit |
|---|---|---|---|---|---|
| DC Supply Voltage (VDD) | | 2.0 | 5.0 | 6.0 | V |
| $V_{IH}$ High-level Input Voltage | VDD=2.0V<br>VDD=4.5V<br>VDD=6.0V | 1.5<br>3.15<br>4.2 | | | V |
| $V_{IL}$ Low-level Input Voltage | VDD=2.0V<br>VDD=4.5V<br>VDD=6.0V | | | 0.5<br>1.35<br>1.8 | V |
| $V_I$ Input Voltage | | 0 | | VDD | V |
| $V_O$ Output Voltage | | 0 | | VDD | V |
| Operating Temperature (TA) | 74HC165 | -40 | | +85 | ℃ |
| | 54HC165 | -55 | | +125 | ℃ |
| Input Rise/Fall Times (tr, tf) | VDD=2.0V<br>VDD=4.5V<br>VDD=6.0V | | | 1000<br>500<br>400 | ns |

**Note**: 2. All unused inputs of the device must be held at VDD or VSS to ensure proper device operation.

**DC ELECTRICAL CHARACTERISTICS**

(Min./Max. limits apply across temperature unless otherwise specified)

| Parameter | Symbol | Typ. | Unit | Guaranteed Limit | VDD | Test Condition | |
|---|---|---|---|---|---|---|---|
| Minimum High Level Output Voltage | $V_{OH}$ | 1.998 | V | 1.9 | 2V | $I_{OH}$=-20μA | $V_I$=$V_{IH}$ or $V_{IL}$ |
| | | 4.499 | | 4.4 | 4.5V | | |
| | | 5.999 | | 5.9 | 6V | | |
| | | 4.3 | | 3.98 | 4.5V | $I_{OH}$=-4mA | |
| | | | | 3.7(54HC) | | | |
| | | | | 3.84(74HC) | | | |
| | | 5.8 | | 5.48 | 6V | $I_{OH}$=-5.2mA | |
| | | | | 5.2(54HC) | | | |
| | | | | 5.34(74HC) | | | |
| Maximum Low Level Output Voltage | $V_{OL}$ | 0.002 | V | 0.1 | 2V | $I_{OL}$=20μA | $V_I$=$V_{IH}$ or $V_{IL}$ |
| | | 0.001 | | | 4.5V | | |
| | | 0.001 | | | 6V | | |
| | | 0.17 | | 0.26 | 4.5V | $I_{OL}$=4mA | |
| | | | | 0.4(54HC) | | | |
| | | | | 0.33(74HC) | | | |
| | | 0.15 | | 0.26 | 6V | $I_{OL}$=5.2mA | |
| | | | | 0.4(54HC) | | | |
| | | | | 0.33(74HC) | | | |
| Maximum Input Current | $I_I$ | ±0.1 | nA | ±100 | 6V | TA=25℃ | VI=VDD or VSS |
| | | | | ±1000 | | | |
| Maximum Supply Current | Icc | - | μA | 8 | 6V | TA=25℃ | VI=VDD or VSS<br>Io=0 |
| | | | | 160(54HC) | | | |
| | | | | 80(74HC) | | | |
| Input Capacitance | $C_{IN}$ | 3 | pF | 10 | 2~6V | | |
| Power Dissipation Capacitance | Cpd | 75 | pF | - | | No load | |

**Timing requirements**

($T_A$=25℃ , $t_r$ = $t_f$ = 6ns)

| Parameter | Symbol | Unit | Guaranteed Limit | 54HC | 74HC | VDD | Test Condition |
|---|---|---|---|---|---|---|---|
| Clock (CK) Frequency | $f_{clock}$ | MHz | 6 | 4.2 | 5 | 2V | |
| | | | 31 | 21 | 29 | 4.5V | |
| | | | 36 | 25 | 15 | 6V | |
| Pulse duration | tw | ns | 80 | 120 | 100 | 2V | SH/LD low |
| | | | 16 | 24 | 20 | 4.5V | OR |
| | | | 14 | 14 | 17 | 6V | CK high or low |
| Setup time | $t_{su}$ | ns | 80 | 120 | 100 | 2V | |
| | | | 16 | 24 | 20 | 4.5V | SH/LD high before CK ↑ |
| | | | 14 | 14 | 17 | 6V | |
| | | | 40 | 60 | 50 | 2V | SER before CK ↑ |
| | | | 8 | 12 | 10 | 4.5V | OR |
| | | | 7 | 10 | 9 | 6V | CLK INH high before CK ↑ |
| | | | 100 | 150 | 125 | 2V | CLK INH low before CK ↑ |
| | | | 20 | 30 | 25 | 4.5V | OR |
| | | | 17 | 26 | 21 | 6V | Data before SH/LD ↓ |
| Hold time | $t_h$ | ns | 5 | 5 | 5 | 2~6V | SER after CK ↑<br>PAR data after SH/LD ↓ |

**AC ELECTRICAL CHARACTERISTICS**

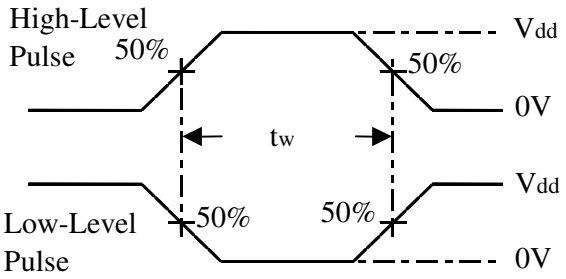
($T_A$=25℃ , $t_r$ = $t_f$ = 6ns, CL=50pF)

| Parameter | Symbol | From (INPUT) | To (OUTPUT) | Typ. | Unit | Guaranteed Limit | 54HC | 74HC | VDD |
|---|---|---|---|---|---|---|---|---|---|
| Maximum Clock (CK) Frequency | $f_{MAX}$ | | | 13 | MHz | 6 | 4.2 | 5 | 2V |
| | | | | 50 | | 31 | 21 | 25 | 4.5V |
| | | | | 62 | | 36 | 25 | 29 | 6V |
| Time Propagation Delay | $t_{pd}$ | SH/LD | $Q_H$ or $\overline{Q}_H$ | 80 | ns | 150 | 225 | 190 | 2V |
| | | | | 20 | | 30 | 45 | 38 | 4.5V |
| | | | | 16 | | 26 | 38 | 32 | 6V |
| | | CK / H | $Q_H$ or $\overline{Q}_H$ | 75 | | 150 | 225 | 190 | 2V |
| | | | | 15 | | 30 | 45 | 38 | 4.5V |
| | | | | 13 | | 26 | 38 | 32 | 6V |
| Transit-time | $t_t$ | | Any | 38 | ns | 75 | 110 | 95 | 2V |
| | | | | 8 | | 15 | 22 | 19 | 4.5V |
| | | | | 6 | | 13 | 19 | 16 | 6V |

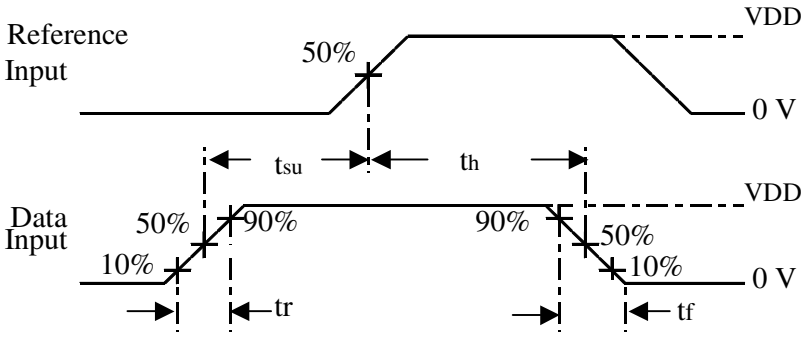
**Note** : 3. $C_{PD}$ determines the no load dynamic power consumption , $P_D=C_{PD}\ VDD^2f + Icc\ VDD$, and the no load dynamic current consumption, $Is = C_{PD}\ VDD^f + Icc$.

**AC SWITCHING WAVEFORM AND AC TEST CIRCUIT**

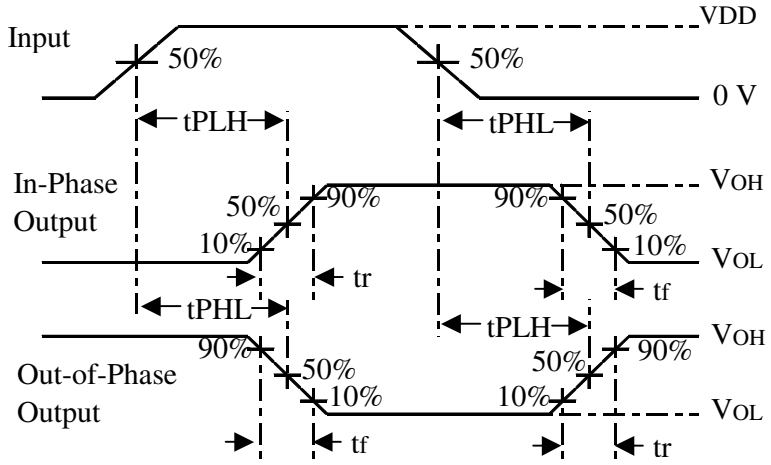
VOLTAGE WAVEFORMS PULSE DURATIONS




VOLTAGE WAVEFORMS SETUP AND HOLD AND INPUT RISE AND FALL TIMES

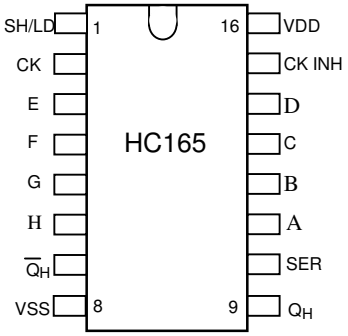



VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



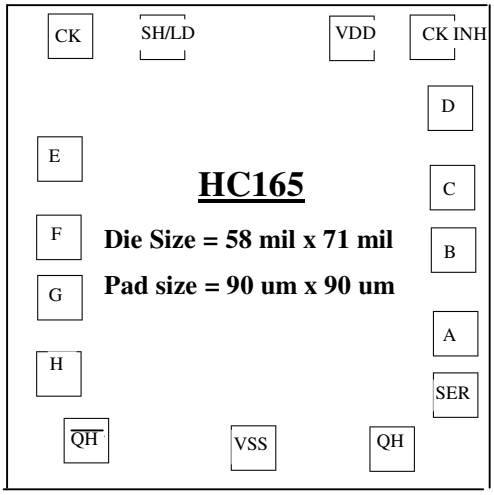
**PIN DESCRIPTION**

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 11,12,13,14,3,4,5,6 | A, B, C, D, E, F, G, H | Data Inputs |
| 7,9 | $\overline{QH}$ , QH | Outputs |
| 8 | VSS | Ground (0V) |
| 2 | CK | Clock input (active at rising edge) |
| 1 | SH/$\overline{LD}$ | Shift load |
| 16 | VDD | Positive power supply |
| 15 | CK INH | Clock inhibit |
| 10 | SER | Serial input |




Pin Configuration

**PAD DIAGRAM**




The Coordinate of Each Pad

| | | | |
|---|---|---|---|
| $\overline{QH}$ | (-361.4, -645.3) | CK INH | (322.1, 539.0) |
| VSS | (-45.4, -645.3) | VDD | (65.3, 539.0) |
| QH | (271.3, -645.3) | SH/LD | (-271.8, 553.5) |
| SER | (342.6, -343.3) | CK | (-432.7, 555.3) |
| A | (342.6, - 200.7) | E | (-432.7, 92.9) |
| B | (342.6, 13.3) | F | (-432.7, -121.1) |
| C | (342.6, 156.1) | G | (-432.7, -270.5) |
| D | (342.6, 370.1) | H | (-432.7, -484.5) |

**Note:** Substrate should be connected to VDD or left it open.