RCL Semiconductors Ltd.

Octal Buffers and Line Drivers with 3-State Outputs HC244

GENERAL DESCRIPTION

The HC244 is fabricated with high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits.

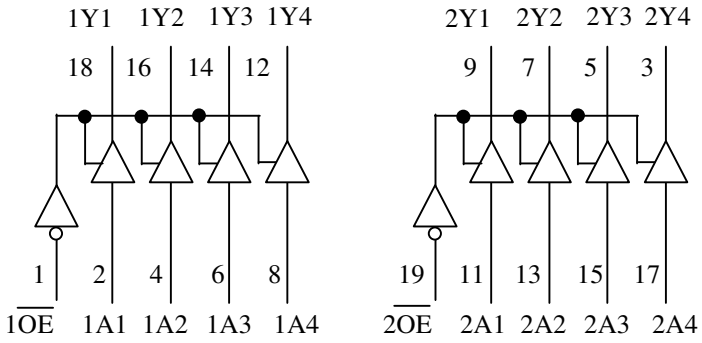
The octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers and bus-oriented receivers and transmitters. HC244 devices are organized as two 4-bit buffers/drivers with separate output-enable (OE) inputs. When $\overline{OE}$ is low, the device passes non-inverted data from A inputs to Y outputs.

When $\overline{OE}$ is high, the outputs are in the high-impedance state.

FEATURES

- Octal buffers and line drivers with 3-state outputs
- Wide operating supply voltage range: 2-6V
- Low input current: < 1•A
- Low quiescent supply current: 80•A max. (74HC series)
- Output Drive at 5V: ±6mA.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Truth Table

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (Vcc)	- 0.5 ~ + 7.0	V
DC input or output Voltage (V_{IN}, V_{OUT})	-0.5 to Vcc +0.5	V
DC Current Drain per pin, any output (I_{out})	±35	mA
Input clamp current, I_{IK} (V1< 0 or V1> Vcc)	±20	mA
Output clamp current , I_{OK} (V0< 0 or V0> Vcc)	±20	mA
DC Current Drain per pin, Vcc or GND (Icc)	±70	mA
Storage Temperature(T_{STG})	-65 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITONS

Parameter		Min.	Normal	Max.	Unit
Vcc Supply Voltage		2	5	6	V
V_{IH} High-level Input Voltage	V_{CC} = 2.0V	1.5			V
	V_{CC} = 4.5V	3.15			
	V_{CC} = 6.0V	4.2			
V_{IL} Low-level Input Voltage	V_{CC} = 2.0V			0.5	V
	V_{CC} = 4.5V			1.35	
	V_{CC} = 6.0V			1.8	
V_I Input Voltage		0		Vcc	V
V_O Output Voltage		0		Vcc	V
Operating Temperature (T_A)	74HC244	-40		85	℃
	54HC244	-55		125	℃
Input Rise/Fall Times (tr, tf)	V_{CC} = 2.0V			1000	ns
	V_{CC} = 4.5V			500	
	V_{CC} = 6.0V			400	

Note: 2. All unused inputs of the device must be held at Vcc or Vss to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions		VDD	T_A = 25℃			54HC245		74HC245		Unit
				Min.	Typ	Max.	Min.	Max.	Min.	Max.	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = -20uA	2.0 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6.0 V	5.9	5.999		5.9		5.9		
		I_{OH} = -6mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = -7.8mA	6.0 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} =20uA	2.0 V		0.002	0.1	0.1		0.1		V
			4.5 V		0.001	0.1	0.1		0.1		
			6.0 V		0.001	0.1	0.1		0.1		
		I_{OL} = 6mA	4.5 V		0.17	0.26	0.4		0.33		
		I_{OL} =7.8mA	6.0 V		0.15	0.26	0.4		0.33		
I_I	V_I = VDD or 0		6.0 V		±0.1	±100	±1000		±1000		nA
I_{OZ}	V_O = VDD or 0		6.0 V		±0.01	±0.5	±10		±5		uA
Icc	V_I = VDD or 0 I_O = 0		6.0 V			8	160		80		uA
Ci			2V ~ 6V		3	10	10		10		pF

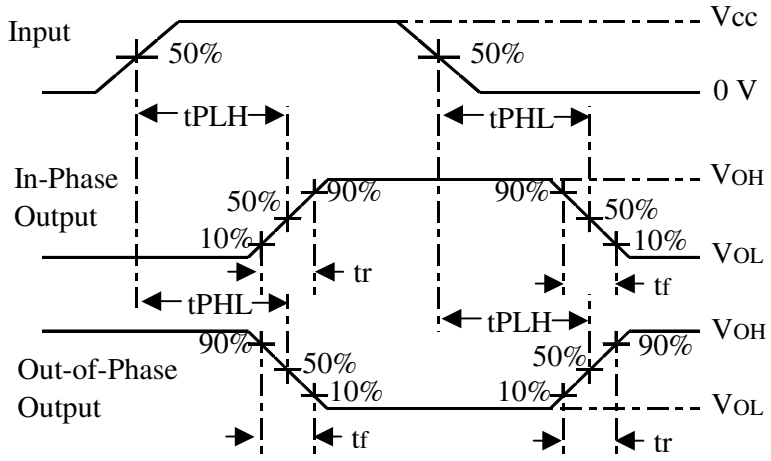
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, unless otherwise noted)(see Figure 1)

Parameter	From (Input)	To (Output)	V_{DD}	T_A = 25℃			54HC245		74HC245		Unit
				Min	Typ	Max	Min	Max	Min	Max	
tpd	A	Y	2.0 V		40	105		170		145	ns
			4.5V		13	23		34		29	
			6.0 V		11	20		29		25	
ten	$\overline{OE}$	Y	2.0 V		75	150		225		190	ns
			4.5V		15	30		45		38	
			6.0 V		13	26		38		32	
tdis	$\overline{OE}$	Y	2.0 V		75	150		225		190	ns
			4.5V		15	30		45		38	
			6.0 V		13	26		38		32	
t_t		Y	2.0 V		28	60		90		75	ns
			4.5V		8	12		18		15	
			6.0 V		6	10		15		13	

AC ELECTRICAL CHARACTERISTICS (C_L=150pF, unless otherwise noted)(see Figure 1)

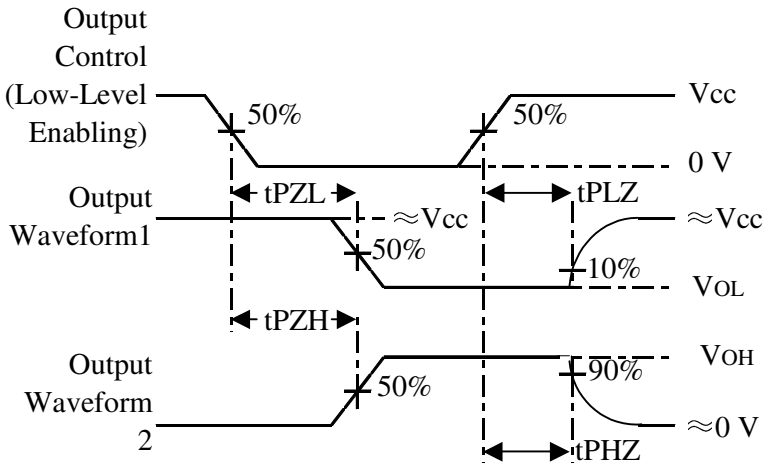
Parameter	From (Input)	To (Output)	V_{DD}	T_A = 25℃			54HC245		74HC245		Unit
				Min	Typ	Max	Min	Max	Min	Max	
tpd	A	Y	2.0 V		56	165		245		210	ns
			4.5V		18	33		49		42	
			6.0 V		15	28		42		35	
ten	$\overline{OE}$	Y	2.0 V		100	200		300		250	ns
			4.5V		20	40		60		50	
			6.0 V		17	34		51		43	
t_t		Y	2.0 V		45	210		315		265	ns
			4.5V		17	42		63		53	
			6.0 V		13	36		53		45	

AC SWITCHING WAVEFORM AND AC TEST CIRCUIT



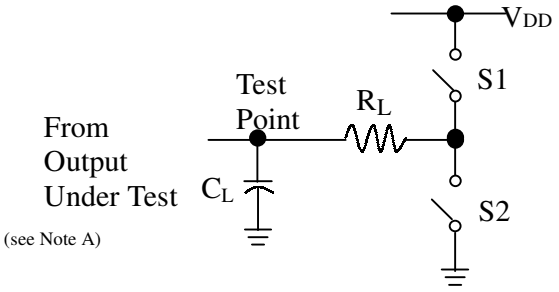
Voltage Waveform
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Voltage Waveform
INPUT RISE AND FALL TIMES



Voltage Waveform
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

Figure 1



Parameter		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
tpd or tt		-	50 pF or 150 pF	Open	Open

Note: 1. CL includes probe and test-fixture capacitance.

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR • 1 MHz, ZO = 50 •, tr = 6 ns, tf = 6 ns.

4. The outputs are measured one at a time with one input transition per measurement.

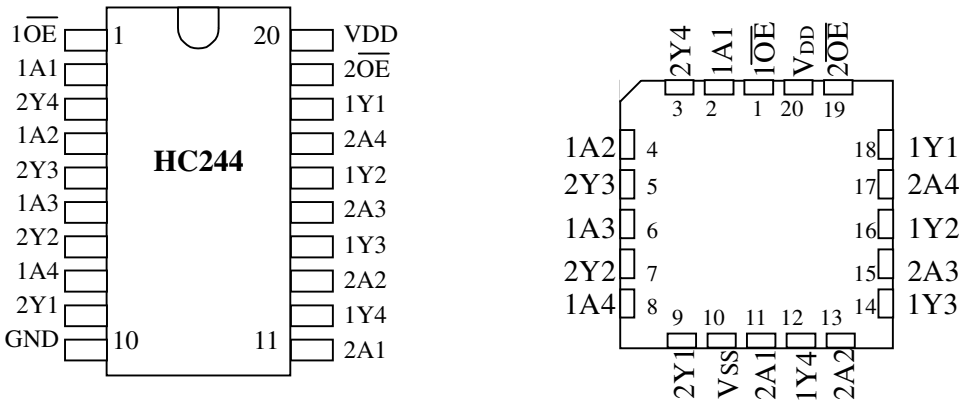
5. tPLZ and tPHZ are the same as tdis.

6. tPZL and tPZH are the same as ten.

7. tPLH and tPHL are the same as tpd.

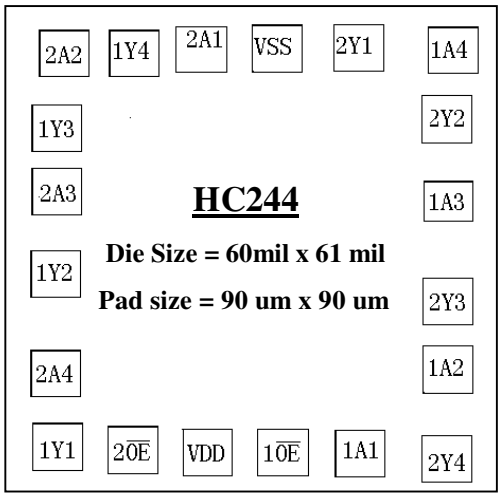
PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1, 19	$1\overline{OE}$, $2\overline{OE}$	Data Inputs
2, 4, 6, 8, 11, 13, 15, 17	1A1 – 1A4, 2A1 – 2A4	Inputs
10	VSS	Ground (0V)
3, 5, 7, 9, 12, 14, 16, 18	2Y4 – 2Y1, 1Y4 – 1Y1	Outputs
14	VDD	Positive power supply



Pin Configuration

PAD DIAGRAM



The Coordinate of Each Pad

1Y1 (-580, -588.3)	1A4(503.8, 523.4)
2$\overline{OE}$ (-303.2, -578.3)	2Y1(288.9, 525.5)
VDD(-121.8, -597.6)	VSS(13.2, 508.8)
1$\overline{OE}$ (100.9, -597.8)	2A1(-127.1, 505.5)
1A1(316.6, - 596.0)	1Y4(-319.8, 515.5)
2Y4(513.7, -597.2)	2A2(-594.0, 24)
1A2(503.8, -352.2)	1Y3(-604.0，183.7)
2Y3（513.7，-178.4）	2A3（-594.0，24.0）
1A3（503.8，99.6）	1Y2（-604.1，-120.7）
2Y2（513.7，246.4）	2A4（-594.0，-392.4）

Note: Substrate should be connected to VDD or left it open.