Preliminary Specification

RCL Semiconductors Ltd.

Octal D-type Flip-Flops With Clear HC273

GENERAL DESCRIPTION

HC273 is fabricated with high-speed silicon gate CMOS technology. It is an octal D-type flip-flop triggered at positive edge of clock (CK). It has a direct clear ($\overline{CL}$).

The data at the data (D) inputs meeting the setup time requirements can be transferred to the Q outputs at the positive edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive pulse. When CK is at either the high or low level, the data at D cannot be transferred to Q.

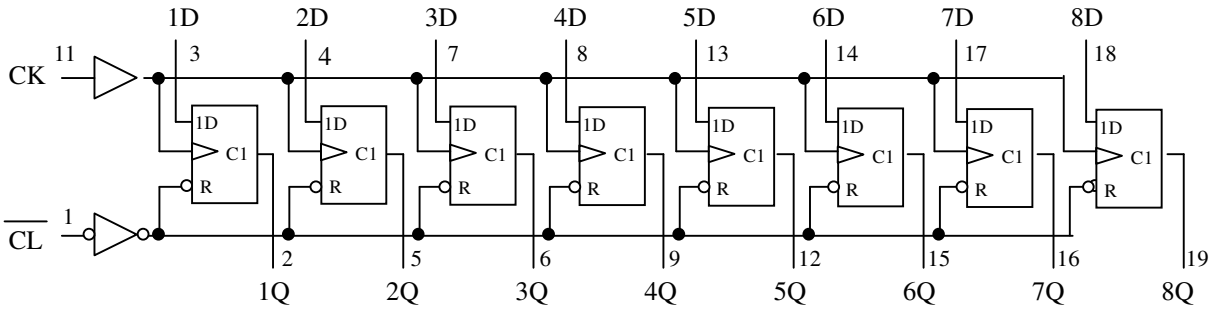
FEATURES

- Contain 8 Flip-Flops with Single-Rail outputs
- Individual data input to each Flip-Flop
- Direct clear input
- Wide operating supply voltage range: 2-6V.
- Low input current: < 1•A.
- Low quiescent supply current: 80 •A maximum.
- Output Drive at 5V: ±4-mA
- Typical propagation delay: 12ns

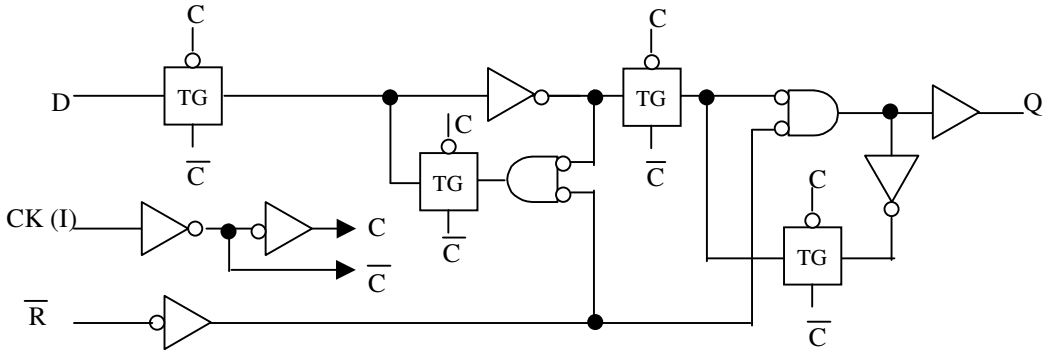
APPLICATION

- Pattern Generators
- Shift Registers
- Buffer/Storage Registers

LOGIC DIAGRAM (Positive Logic)



LOGIC DIAGRAM FOR EACH D FLIP-FLOP (Positive Logic)



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FUNCTIONAL DESCRIPTION

Truth Table

INPUTS			OUTPUT
CL	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Qo

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (VDD)	- 0.5 ~ + 7.0	V
DC Current per output pin (I_{oL} or I_{oH})	±25	mA
DC Current VDD or GND (Icc)	±50	mA
Storage Temperature(T_{STG})	-65 ~ +150	℃
Lead Temperature (T_L)		℃

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITONS

Symbol & Parameter			Min.	Normal	Max.	Unit
VDD	Supply voltage		2	5	6	V
V_{IH}	High-level Input Voltage	VDD=2.0V	1.5			V
		VDD=4.5V	3.15			
		VDD=6.0V	4.2			
V_{IL}	Low-level Input Voltage	VDD=2.0V			0.5	V
		VDD=4.5V			1.35	
		VDD=6.0V			1.8	
V_I	Input Voltage		0		VDD	V
V_O	Output Voltage		0		VDD	V
T_A	Operating Temperature	74HC	-40		85	℃
		54HC	-55		125	℃
tr, tf	Input Rise/Fall Times	VDD=2.0V			1000	ns
		VDD=4.5V			500	
		VDD=6.0V			400	

Note: 2. All unused inputs of the device must be held at VDD or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS (unless otherwise specified)

PARAMETER	TEST CONDITIONS		VDD	TA = 25℃ MIN	TYP	MAX	54HC595 MIN	MAX	74HC595 MIN	MAX	UNIT
V_{OH}	V_I= V_{IH} or V_{IL}	I_{OH} = -20uA	2 V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = -4 mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH} = -5.2mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} = 20uA	2 V		0.002	0.1	0.1		0.1		V
			4.5V		0.001	0.1	0.1		0.1		
			6 V		0.001	0.1	0.1		0.1		
		I_{OL} = 4 mA	4.5V		0.17	0.26	0.4		0.33		
		I_{OL} = 5.2mA	6 V		0.15	0.26	0.4		0.33		
I_I	V_I = VDD or 0		6 V		±0.1	±100		±1000		±1000	nA
Icc	V_I = VDD or 0 I_O = 0		6 V			8		160		80	uA
Ci			2V ~ 6V		3	10		10		10	pF

TIMING REQUREMENTS OVER RECOMMENED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

PARAMETER			VDD	T_A = 25℃ MIN	MAX	54HC MIN	MAX	74HC MIN	MAX	UNIT
f_{clock}	Clock frequency		2 V		5		4		4	MHz
			4.5V		27		18		21	
			6 V		32		21		25	
tw	Pulse duration	$\overline{CL}$ low	2 V	80		120		100		
			4.5V	16		24		20		ns
		CK high or low	6 V	14		20		17		
tsu	Setup time before CK ↑	Data	2 V	100		150		125		ns
			4.5V	20		30		25		
			6 V	17		25		21		
		$\overline{CL}$ inactive	2 V	100		150		125		
			4.5V	20		30		25		
			6 V	17		25		21		
th	Hold time, data after CK ↑			0		0		0		ns

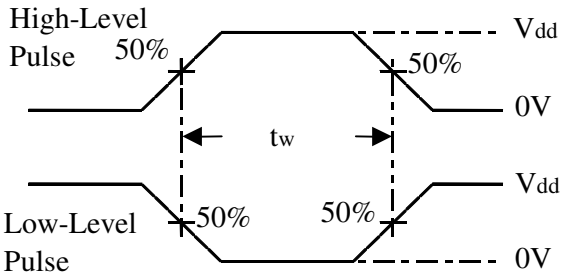
AC ELECTRICAL CHARACTERISTICS (T_A =25℃ , t_r = t_f =6ns, C_L=50 pF)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VDD	T_A = 25℃ MIN	TYP	MAX	54HC MIN	MAX	74HC MIN	MAX	UNIT
fmax			2 V	5	11		4		4		MHz
			4.5V	27	50		18		21		
			6 V	32	60		21		25		
t_{PHL}	$\overline{CL}$	Any	2 V		55	160		240		200	ns
			4.5V		15	32		48		40	
			6 V		12	27		41		34	
t_{pd}	CK	Any	2 V		56	160		240		200	ns
			4.5V		15	32		48		40	
			6 V		13	27		41		34	
t_t		Any	2 V		38	75		110		95	ns
			4.5V		8	15		22		19	
			6 V		6	13		19		16	

AC SWITCHING WAVEFORM

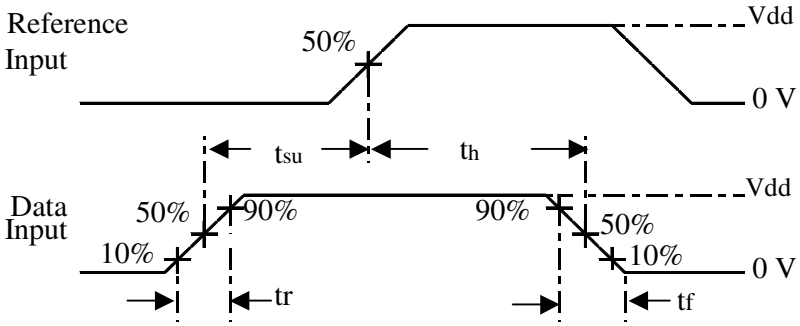
Waveform 1:

Voltage Waveform Pulse Duration



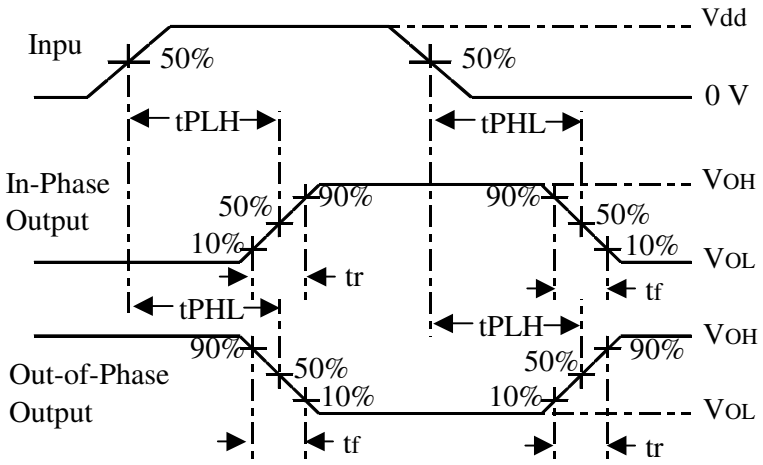
Waveform 2:

Setup and hold time
Input rise and fall times



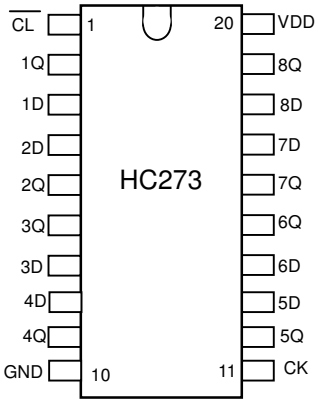
Waveform 3:

Propagation Delay
And Output transition
Times



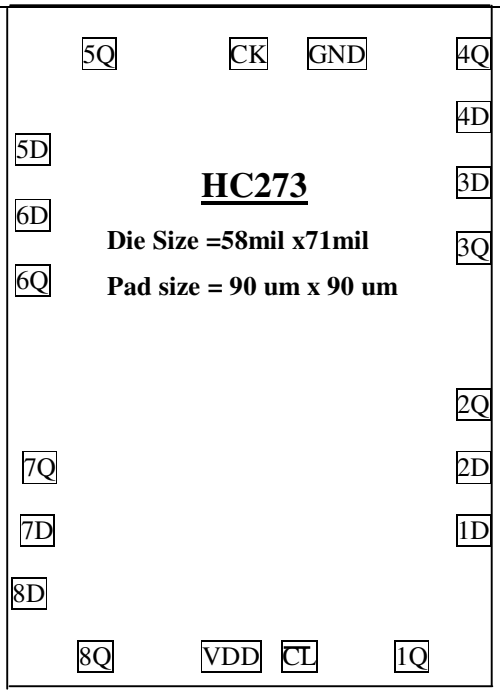
PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
3, 4, 7, 8, 13, 14, 17, 18	1D–8D	Data Inputs
2, 5, 6, 9, 12, 15, 16, 19	1Q – 8Q	Outputs
10	GND	Ground (0V)
11	CK	Clock input (active at rising edge)
1	$\overline{CL}$	Master reset input (active at Low)
20	VDD	Positive power supply



Pin Configuration

PAD DIAGRAM



The Coordinate of Each Pad

1Q	(339.3 , -749.4)	5Q	(-417.6 , 669.9)
2Q	(403.1 , -239.6)	6Q	(-496.6 , 109.4)
3Q	(403.8 , 170.9)	7Q	(-496.6 , -303.1)
4Q	(358.5 , 686.3)	8Q	(-420.7 , -748.4)
1D	(384.4 , -520.3)	5D	(-478.7 , 445.6)
2D	(384.4 , -379.9)	6D	(-478.7 , 304.8)
3D	(384.4 , 311.1)	7D	(-478.7 , -443.2)
4D	(384.4 , 451.9)	8D	(-478.7 , -584.1)
GND	(46.0 , 670.7)	VDD	(-137.8 , -749.4)
$\overline{CL}$	(24.7 , -745.1)	CK	(-143.3 , 672.4)

Note: Substrate should be connected to VDD or left it open.