Preliminary Specification

RCL Semiconductors Ltd.

Tri–State Octal Transparent D-Type Latch HC573

GENERAL DESCRIPTION

HC573 is fabricated in the high speed-silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

This 8-bit transparent D-type latch with 3-state outputs is specifically designed for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

When the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (H or L logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

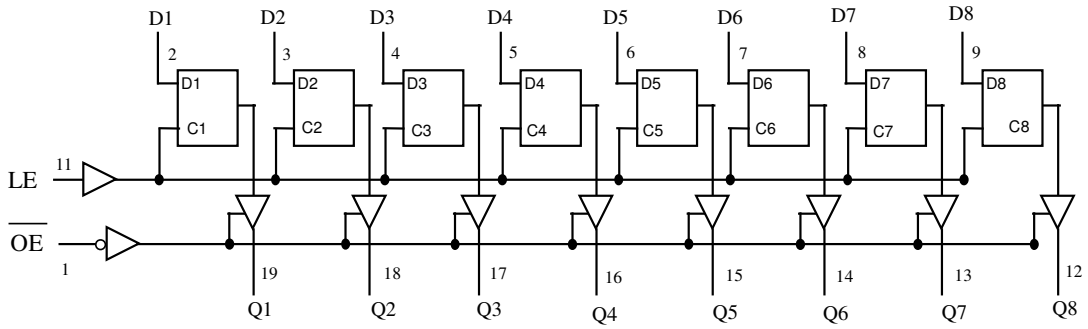
$\overline{OE}$ should be tied to V_{DD} through a pull-up resistor to ensure the high-impedance state during power up or power down; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FEATURES

- Wide operating supply voltage range: 2-6V
- Output Drive at V_{DD} = 5V : ±6mA
- Typical propagation delay: 21ns
- Low input current: < 1μA.
- Low quiescent supply current: 80μA maximum
- Bus-Structured Pinout
- High-Current 3-state outputs drive bus lines
- Customer-Specific Configuration Control can be supported along with Major-change approval
- Qualified for Automotive Applications

LOGIC DIAGRAM



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FUNCTIONAL DESCRIPTION

Truth Table

Inputs			Output Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	LE	X	Q_0
H	X	X	Z

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)
Z = high impedance state
Q_0= The level of the output before steady state input conditions were established

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (V_{DD})	- 0.5 ~ + 7.0	V
DC input or output Voltage (VIN, VOUT)	-0.5 to V_{DD} +0.5	V
DC Current Drain per pin, any output (Iout)	±35	mA
DC Current Drain per pin, V_{DD} or GND (Icc)	±70	mA
Storage Temperature(TSTG)	-65 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Normal	Max.	Unit
DC Supply Voltage (V_{DD})		2.0	5.0	6.0	V
VIH High-level Input Voltage	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V	1.5 3.15 4.2			V
VIL Low-level Input Voltage	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V			0.5 1.35 1.8	V
VI Input Voltage		0		V_{DD}	V
VO Output Voltage		0		V_{DD}	V
Operating Temperature (T_A)		-40		+125	℃
t_t Input transition time (rise and fall)	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V			1000 500 400	ns

Note: 2. All unused inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS (unless otherwise specified)

Parameter	Test Conditions		V_{DD}	TA =25°C			TA = -40°C ~125°C		TA = -40°C ~85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	V_I=V_{IH} or V_{IL}	I_{OH}= -20μA	2.0V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6.0V	5.9	5.999		5.9		5.9		
		I_{OH}= -6mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH}= -7.8mA	6.0V	5.48	5.8		5.2		5.34		
V_{OL}	V_I=V_{IH} or V_{IL}	I_{OL} = 20μA	2.0V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6.0V		0.001	0.1		0.1		0.1	
		I_{OL} = 6mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8mA	6.0V		0.15	0.26		0.4		0.33	
I_I	V_I=V_{DD} or 0		6.0V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O =V_{DD} or 0		6.0V		±0.01	±0.5		±10		±5	μA
Icc	V_I=V_{DD} or 0	I_O =0	6.0V			8		160		80	μA
Ci			2~6V		3	10		10		10	pF

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING TEMPERATURE RANGE (unless otherwise noted)

Parameter	V_{DD}	TA =25°C		TA = -40°C ~125°C		TA = -40°C ~85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_w Pulse duration, LE high	2.0V	80		120		100		ns
	4.5V	16		24		20		
	6.0V	14		20		17		
t_{su} Setup time, data before LE↓	2.0V	50		75		63		ns
	4.5V	10		15		13		
	6.0V	9		13		11		
t_h Hold time, data after LE↓	2.0V	20		24		24		ns
	4.5V	5		5		5		
	6.0V	5		5		5		

AC ELECTRICAL CHARACTERISTICS (CL = 50pF)

Parameter	From (Input)	To (Output)	VDD	TA =25°C			TA = -40°C ~125°C		TA = -40°C ~85°C		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
t_{pd}	D	Q	2.0V		77	175		265		220	ns
			4.5V		26	35		53		44	
			6.0V		23	30		45		38	
	LE	Any Q	2.0V		87	175		265		260	ns
			4.5V		27	35		53		44	
			6.0V		23	30		45		38	
t_{en}	$\overline{OE}$	Any Q	2.0V		68	150		225		190	ns
			4.5V		24	30		45		38	
			6.0V		21	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2.0V		47	150		225		190	ns
			4.5V		23	30		45		38	
			6.0V		21	26		38		32	
t_t		Any Q	2.0V		28	60		90		75	ns
			4.5V		8	12		18		15	
			6.0V		6	10		15		13	

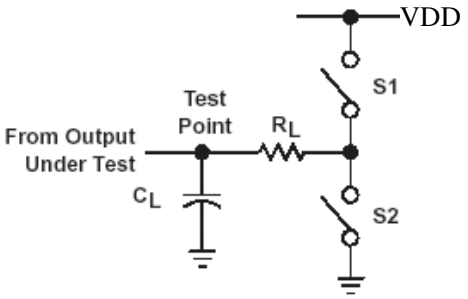
AC ELECTRICAL CHARACTERISTICS (CL = 150pF)

Parameter	From (Input)	To (Output)	VDD	TA =25°C			TA = -40°C ~125°C		TA = -40°C ~85°C		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
t_{pd}	D	Q	2.0V		95	200		300		250	ns
			4.5V		33	40		60		50	
			6.0V		21	34		51		43	
	LE	Any Q	2.0V		103	225		335		285	ns
			4.5V		33	45		67		57	
			6.0V		29	38		57		48	
t_{en}	$\overline{OE}$	Any Q	2.0V		85	200		300		250	ns
			4.5V		29	40		60		50	
			6.0V		26	34		51		43	
t_t		Any Q	2.0V		60	210		315		265	ns
			4.5V		17	42		63		53	
			6.0V		14	36		53		45	

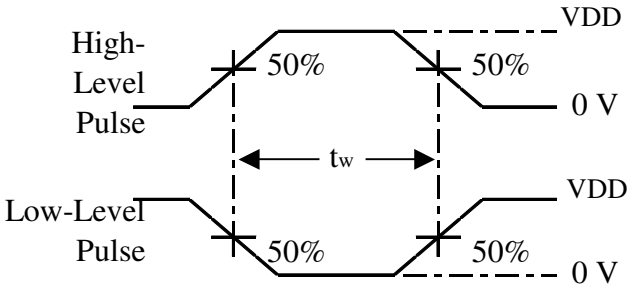
Parameter		Test Conditions	Typ.	Unit
C_{PD}	Power Disspation Capitance	TA =25°C , No Load	50	pF

Note 3: C_{PD} determines the no load dynamic power consumption , $P_D=C_{PD}\cdot V_{DD}^2\cdot f + Icc \cdot V_{DD}$, and the no load dynamic current consumption, $Is = C_{PD}\cdot V_{DD}\cdot f_i + Icc$

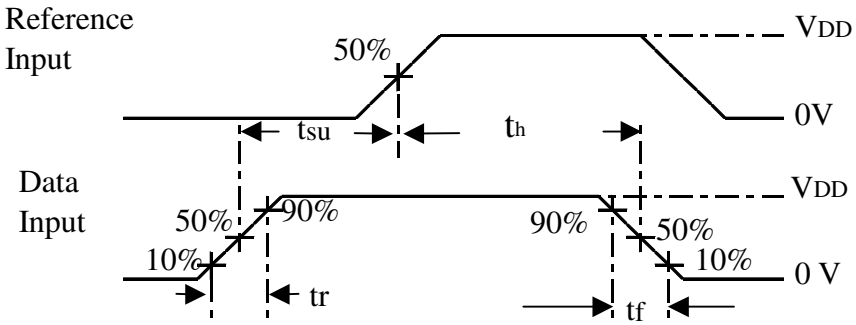
AC TEST CIRCUIT AND AC SWITCHING WAVEFORM



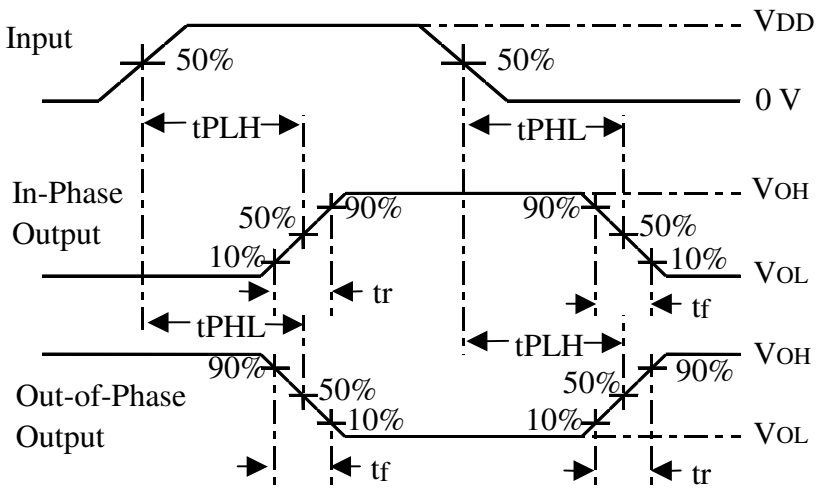
PARAMETER		R_L	C_L	S1	S2
ten	t_{PZH}	1kΩ	50pF or 150pF	Open	Closed
	t_{PZL}			Closed	Open
tdis	t_{PHZ}	1kΩ	50pF	Open	Closed
	t_{PLZ}			Closed	Open
tpd or t_t		---	50pF or150pF	Open	Open



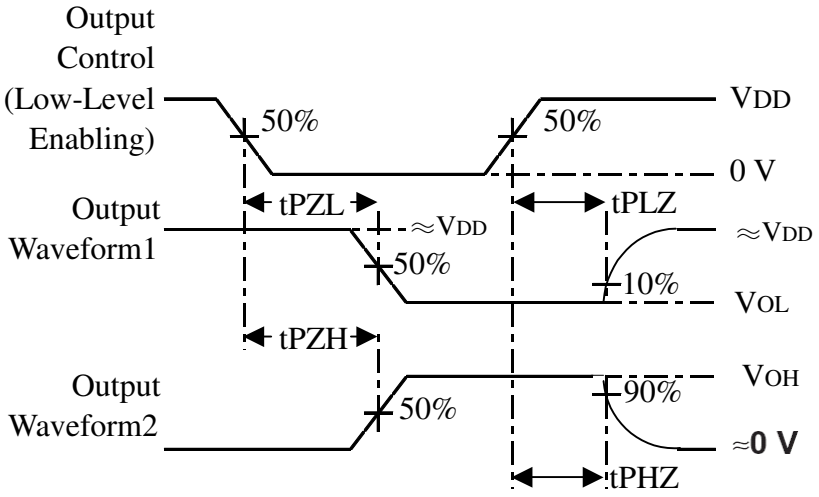
Voltage Waveforms
Pulse Durations



Voltage Waveforms
Setup and Hold and Input Rise and Fall times



Voltage Waveforms
Propagation Delay and Output Transition Times



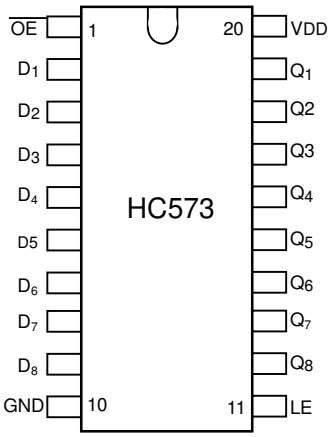
Voltage Waveforms
Enable and disable times for 3-state outputs

NOTES 4:

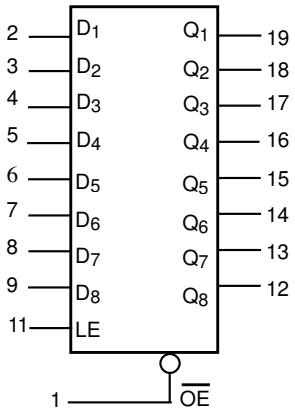
1) C_L includes probe and test-fixture capacitance.
2) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3) Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:
   PRR ≤ 1 MHz, Z_O = 50Ω, t_r = 6 ns, t_f = 6 ns.
4) The outputs are measured one at a time, with one input transition per measurement.
5) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6) t_{PZL} and t_{PZH} are the same as t_{en}.
7) t_{PLH} and t_{PHL} are the same as t_{pd}.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
2 - 9	D1– D8	Data Inputs
12 - 19	Q8 – Q1	Outputs
10	GND	Ground (0V)
11	$\overline{LE}$	Latch-enable input
1	$\overline{OE}$	Buffered output-enable
20	V_{DD}	Positive power supply

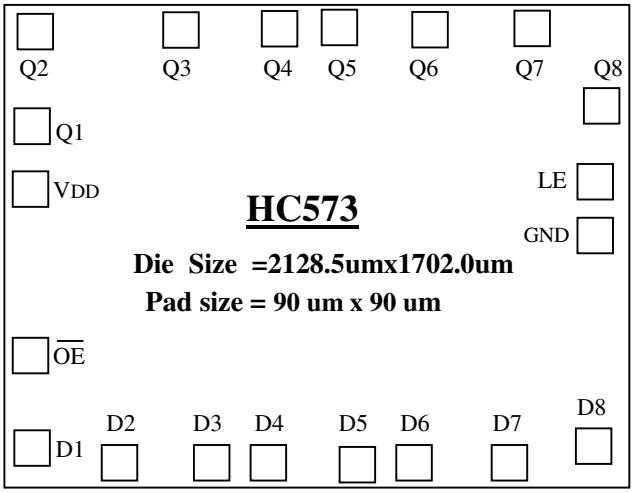


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

D1 (-768.3,-555.9)	Q8 (681.3, 313.6)
D2 (-546.5, -594.1)	Q7 (502.1, 510.7)
D3 (-309.0, -594.4)	Q6 (246.0, 510.8)
D4 (-168.5, -594.2)	Q5 (13.6, 510.9)
D5 (60.6, -594.1)	Q4(-134.3, 510.9)
D6 (203.3, -594.0)	Q3 (-389.4, 510.9)
D7 (449.0, -594.1)	Q2 (-760.7, 501.7)
D8 (660.5, -548.1)	Q1 (-766.3, 265.6)
GND (663.5, -16.8)	VDD (-772.7, 106.4)
LE (666.3, 123.7)	$\overline{OE}$ (-772.7, -323.5)

Note: Substrate should be connected to VDD or left it open.

PAD IDENTIFICATION