Preliminary Specification

RCL Semiconductors Ltd.

Dual D Flip-Flops with Preset and Clear HC74

GENERAL DESCRIPTION

HC74 is fabricated with high speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits.

The HC74 devices contain two independent D-type flip-flops triggered at the positive edge of Clock (CK). A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

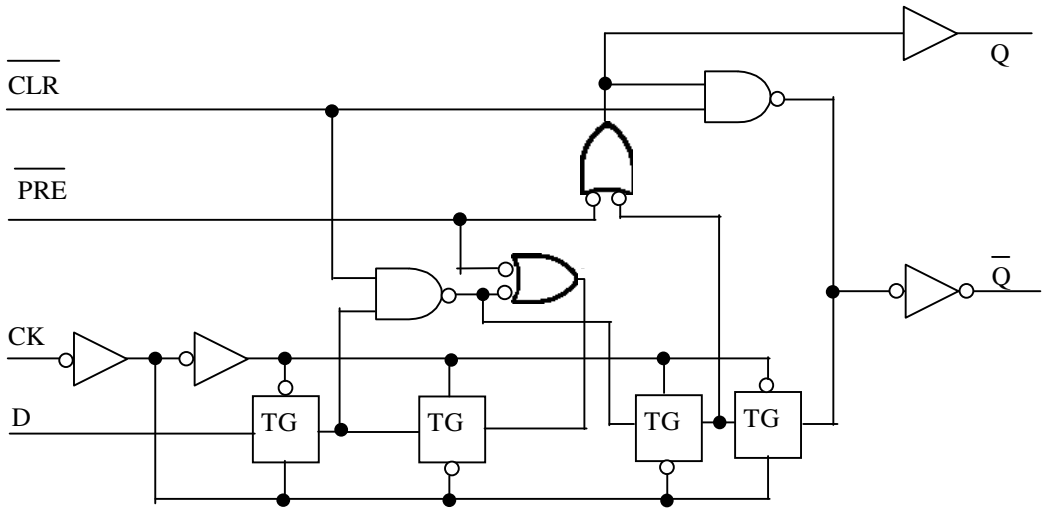
The HC74 utilizes silicon gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data , preset, clear, clock inputs, Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

FEATURES

- Output Drive at 5V: ±4-mA
- Typical propagation delay: 15ns
- Wide operating supply voltage range: 2-6V.
- Low input current: < 1μA.
- Low quiescent supply current: 40-μA maximum.
- Fanout of 10 LS-TTL Loads.

LOGIC DIAGRAM



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FUNCTIONAL DESCRIPTION

1. Truth Table

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level.

Note: Q0= the level of Q before the indicated input conditions were established.
*: This configuration is non-stable; that is, it will not persist when preset and clear inputs return to their inactive(high) level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Supply voltage (VDD)	- 0.5 ~ + 7.0	V
Input clamp current , I_{IK} (V1 < 0 or V1> VDD)	±20	mA
Output clamp current , I_{OK} (V0 < 0 or V0> VDD)	±20	mA
Continuous output current , Io (Vo = 0 to VDD)	±25	mA
Continuous current through VDD or VSS	±50	mA
Storage temperature range , T_{stg}	-65 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Normal	Max.	Unit
DC Supply Voltage (VDD)		2.0	5.0	6.0	V
V_{IH} High-level Input Voltage	VDD=2.0V VDD=4.5V VDD=6.0V	1.5 3.15 4.2			V
V_{IL} Low-level Input Voltage	VDD=2.0V VDD=4.5V VDD=6.0V	F		0.5 1.35 1.8	V
V_I Input Voltage		0		VDD	V
V_O Output Voltage		0		VDD	V
Operating Temperature (TA)	74HC74	-40		+85	℃
	54HC74	-55		+125	℃
Input Rise/Fall Times (tr, tf)	VDD=2.0V VDD=4.5V VDD=6.0V			1000 500 400	ns

Note: 2. All unused inputs of the device must be held at VDD or VSS to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

(T_A =25℃)

Parameter	Symbol	Unit	Typ.	Guaranteed Limit	VDD	Test Condition	
Minimum High Level Output Voltage	V_{OH}	V	VDD-0.002	VDD-0.1	2V	I_{OH} = -20 μ A	V_I = V_{IH} or V_{IL}
			VDD-0.001	VDD-0.1	4.5~6V		
			4.3	3.98	4.5V	I_{OH} = -4 mA	
				3.7		(54HC)	
				3.84		(74HC)	
			5.8	5.48	6V	I_{OH} = -5.2mA	
				5.2		(54HC)	
				5.34		(74HC)	
Maximum Low Level Output Voltage	V_{OL}	V	0.002	0.1	2V	I_{OL} = 20 μ A	V_I = V_{IH} or V_{IL}
			0.001	0.1	4.5~6V		
			0.17	0.26	4.5V	I_{OL} = 4 mA	
				0.4		(54HC)	
				0.33		(74HC)	
			0.15	0.26	6V	I_{OL} = 5.2 mA	
				0.4		(54HC)	
				0.33		(74HC)	
Maximum Input Current	I_I	nA	±0.1	±100	6V	(54/74HC)	V_I = VDD or 0
				±1000			
Maximum Supply Current	Icc	μ A	-	2	6V	V_I = VDD or 0	I_O = 0
				40	(54HC)		
				20	(74HC)		
	Ci	pF	3	10	2V~6V		
Power Dissipation capacitance per FLIP-FLOP	Cpd	pF	35			No load	

AC ELECTRICAL CHARACTERISTICS(timing requirements)

(C_L=50pF, T_A =25℃)

Parameter		Symbol	Unit	Guaranteed Limit	54HC	74HC	VDD
Clock frequency		fclock	MHz	6	4.2	5	2V
				31	21	25	4.5V
				36	25	29	6V
Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	tw	ns	100	150	125	2V
				20	30	25	4.5V
				17	25	21	6V
	CK high or low			80	120	100	2V
				16	24	20	4.5V
				14	20	17	6V
Setup time before CK ↑	Data	tsu	ns	100	150	125	2V
				20	30	25	4.5V
				17	25	21	6V
	$\overline{PRE}$ or $\overline{CLR}$ inactive			25	40	30	2V
				5	8	6	4.5V
				4	7	5	6V
Hold time, data after CK ↑		th	ns	0	0	0	2~6V

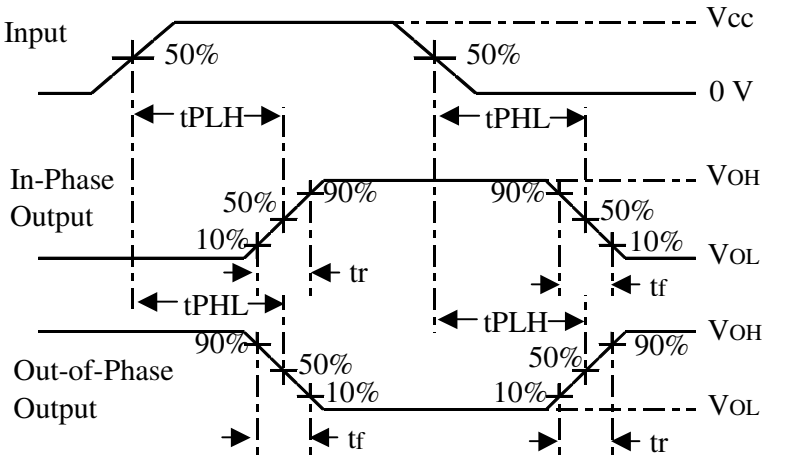
AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Guaranteed Limit	54HC	74HC	VDD	From	To
Maximum	fmax	10	MHz	6	4.2	5	2V		
Clock		50		31	21	25	4.5V		
Frequency		60		36	25	29	6V		
	t_{pd}	70	ns	230	345	290	2V	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$
		20		46	69	58	4.5V		
		15		39	59	49	6V		
		70		175	250	220	2V	CK	Q or $\overline{Q}$
		20		35	50	44	4.5V		
		15		30	42	37	6V		
transmit	t_t	28	ns	75	110	95	2V		Q or $\overline{Q}$
time		8		15	22	19	4.5V		
		6		13	19	16	6V		

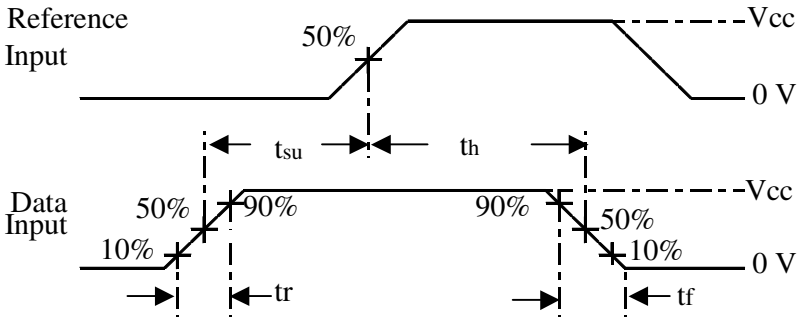
Note : 3. C_{PD} determines the no load dynamic power consumption , $P_D=C_{PD}\ VDD^2f$ + Icc VDD, and the no load dynamic current consumption, $Is = C_{PD}\ VDD^f$ + Icc.

AC SWITCHING WAVEFORM AND AC TEST CIRCUIT

VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



INPUT RISE AND FALL TIMES



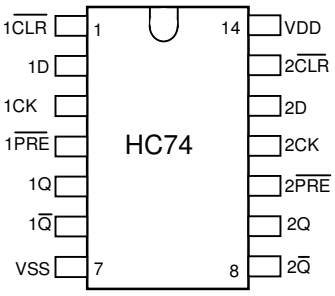
Notes: a. CL includes probe and test-fixture capacitance.

b. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics : PRR≤1MHz , Zo=50Ω, tr=tf=6ns.

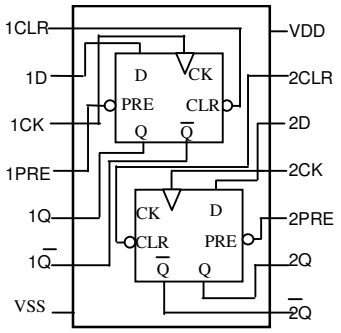
c. The outputs are measured one at a time with one input transition per measurement. t_{PLH} and t_{PHL} are the same as tpd.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
2, 12	1D, 2D	Data Inputs
5, 6, 8, 9	1Q, 1$\overline{Q}$, 2$\overline{Q}$, 2Q	Outputs
7	VSS	Ground (0V)
3, 11	1CK, 2CK	Clock input
1, 13	1$\overline{CLR}$, 2$\overline{CLR}$	Clear
4, 10	1$\overline{PRE}$, 2$\overline{PRE}$	PRESET
14	VDD	Positive power supply

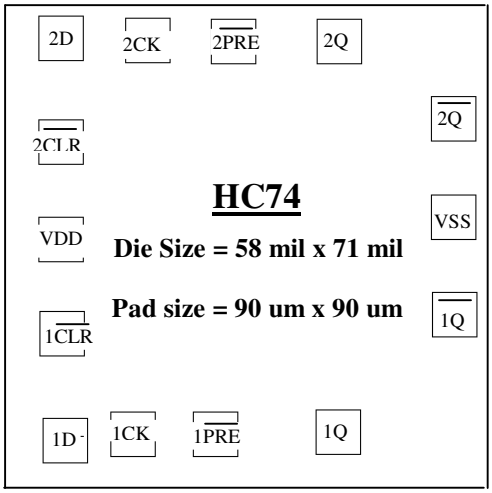


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

1D (-425.5, 450.3)	2Q (106.5, 355.9)
1CK (-284.1, -445.9)	2$\overline{PRE}$ (-142.9, 355.9)
1$\overline{PRE}$ (-142.9,-445.9)	2CK (-284.1, 355.9)
1Q (106.9, -445.9)	2D (-425.5, 360.3)
1$\overline{Q}$ (351.4, -298.4)	2$\overline{CLR}$ (-425.7,114.3)
VSS (351.4,- 45.0)	VDD (-423.5, -46.1)
2$\overline{Q}$ (351.4, 208.4)	1$\overline{CLR}$ (-425.5, -204.3)

Note: Substrate should be connected to VDD or left it open.