RCL Semiconductors Ltd.

EL Lamp Driver IC C1001A

GENERAL DESCRIPTION

The C1001A series product is a poly gate CMOS integrated circuit which is designed to drive an Electoluminescence Lamp (EL) to light. It supplies three pins for trigger input: one is active at low (ALM) and other two are active at high (TG & FLSH). 3 seconds display delay function is implemented by internal divider. Only ALM and TG will generate 3 seconds delay but FLSH not. The switching and EL driving frequency is decided by an internal RC oscillator. The driving capability for IND output and frequency for EL output are different options, the detail information shown in the OPTION LIST.

C1001A series product can be widely used in the back light of digital watch, analogy watch, calculator etc.

FUNCTIONS

- Single 3V or 1.5V battery operation.
- DC to AC conversion.
- Built-in RC oscillator.
- Built-in delay function.
- Three independent trigger inputs:
  ALM (L) makes EL display for 3 second delay.
  TG (H) makes EL display for 3 second delay.
  FLSH (H) makes EL flash companied with the pluse from FLSH without any delay .
  (See Timing Diagram)

FEATURES

- Economical solution for EL display.
- CMOS process and low power consumption.
- No external component needed for delay function.
- Min. external components application.

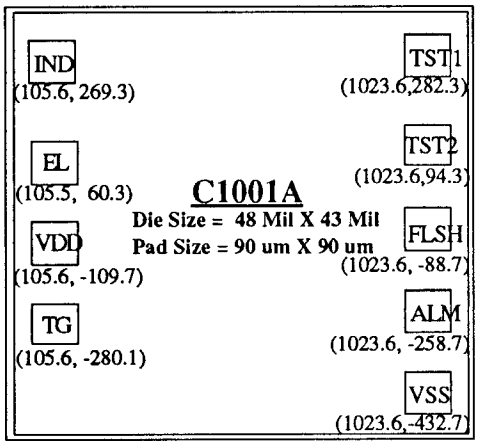
OPTION LIST

OPTION	IND Ouput Current IOH1 (ma)			Oscillator Frequency Fosc (KHz)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
C1001A	0.25	0.5	-	170	240	310
C1001A2	1.0	1.5	-	400	500	670
C1001A3	0.2	0.4	-	400	500	670

COIL OPTION LIST FOR C1001A-2

VDD (V)	Coil		EL Area (cm squ.)	EL Voltage (V)
	MH	OHM		
3.0	3	22	1.2 X 2.4	140
	2	14	2.5 X 2.5	120
	1.6	14	2.5 X 2.5	140
	1.0	10	4.0 X 4.0	120
	0.8	9	5.0 X 5.0	90
1.5	2	14	1.5 X 2.5	100

PAD ASSIGNMENT AND PIN DESCRIPTION



PIN	DESCRIPTION
IND	DC to AC converter output
EL	DC to AC converter output
VDD	Positive power supply
TG	Trigger input pin active at high
TST1, TST2	Test Pins
FLSH	Trigger input pin active at high
ALM	Trigger input pin active at low
Vss	Negative power supply

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ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Parameter	Symbol	Limits
Power supply voltage range	V_{DD} - V_{SS}	- 0.3V to + 5.0V
Input voltage range	Vin	V_{SS} - 0.3 to V_{DD} + 0.3
Operating temperature range	T_A	0 to +60°C
Storage temperature range	Tstg	-40 to +70°C

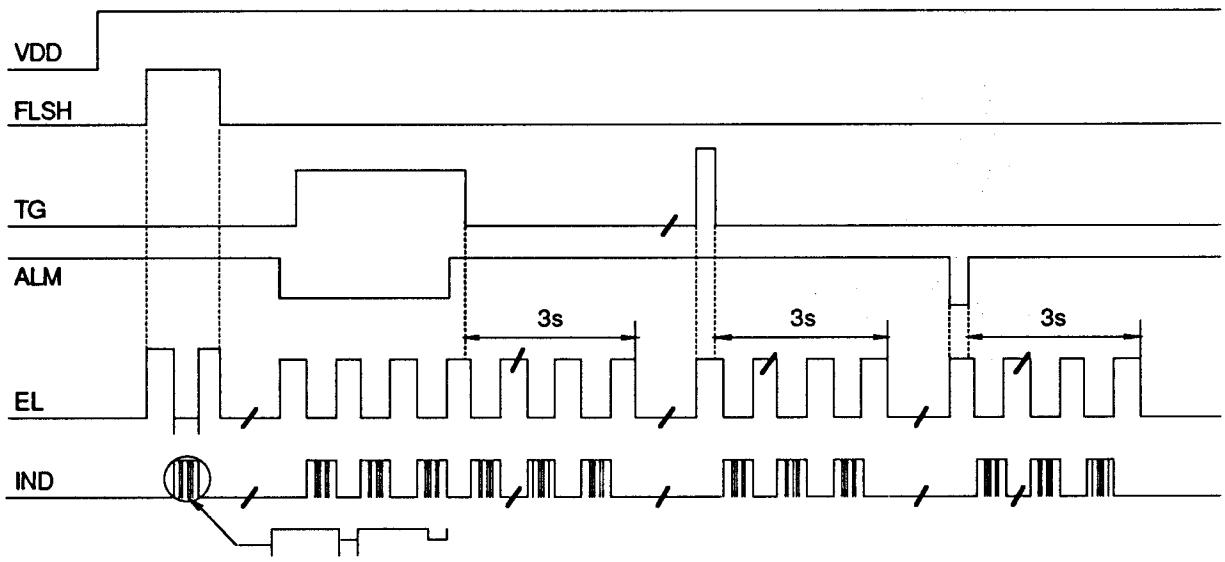
DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, Ta = 25°C, V_{DD} = 3.0V, Vss = 0V

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating voltage range	V_{DD}	1.3	3.0	4.5	V	—
Standard current	I_{DD}	--	0.1	1	μA	*no load
IND Output Source Current	I_{OH1}	0.2	0.4	**0.7	mA	V_{OH} = 0.8V
EL Output Source Current	I_{OH2}	0.2	0.6	--	mA	V_{OH} = 0.8V
IND Ouput Sink Current	I_{OL1}	10	20	--	mA	V_{OL} = 0.8V
EL Ouput Sink Current	I_{OL2}	0.5	2	--	mA	V_{OL} = 0.8V
Oscillator Starting Voltage	V_{STP}	1.3	--	--	V	—
Oscillator Frequency	***Fosc	400	500	670	KHZ	V_{DD} = 3.0V

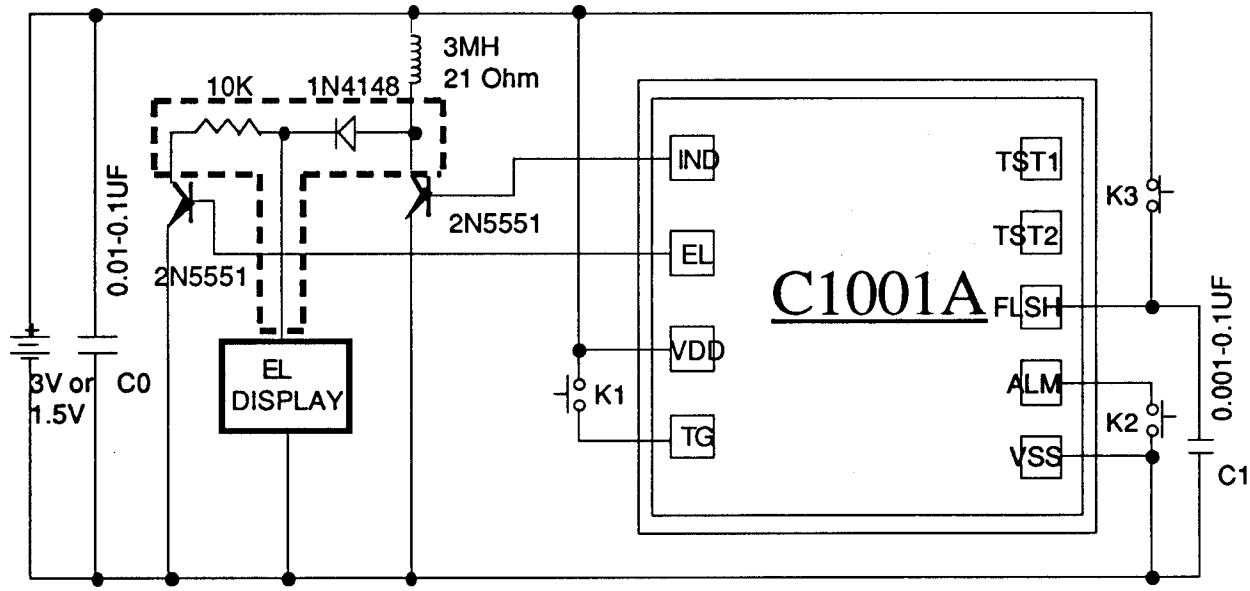
Note: * refers to EL & IND open, all trigger input open.
** The Max. IND source current IOH1 can be enlarged to 4 ma by mask option. The value in the above table refers to C1001A3 OPTION. Others can be found in the OPTION LIST.
*** The parameter Fosc in the above table refers to option C1001A3. Others can be found in the OPTION LIST.

TIMING DIAGRAM



TYPICAL APPLICATION CIRCUIT

(Selection of K1, K2 AND K3 for different applications)

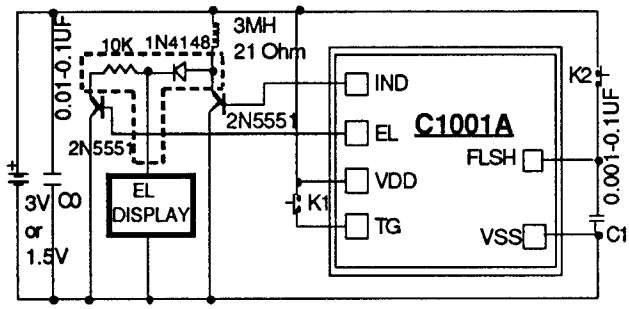


NOTE:

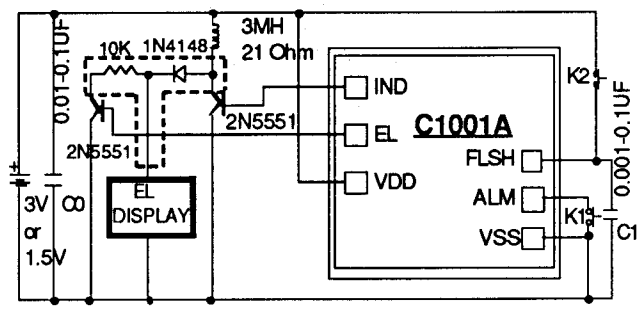
1. **Substrate is connector to VDD.**
2. **The wires connected to TG and ALM cannot across the lines inside the black dote line box. Furthermore, these wires should be separated from the lines inside the black dote line box by Vss or Vdd.**
3. **The capacitor C1 can be connected to Vss or Vdd.**
4. **During the watch application, the two wires connected to crystal are better to be surrounded by Vss or Vdd, and they are the farer the better away from the wire connected to EL.**
5. **The items 2, 3, 4 are very important for PCB layout. The above items are also applied to the following applications (A-H) and will not be rementioned again.**

ALL KINDS OF APPLICATION CIRCUIT

A. Application with 3 Second Delay using Vdd Trigger & without Delay using FLSH Trigger

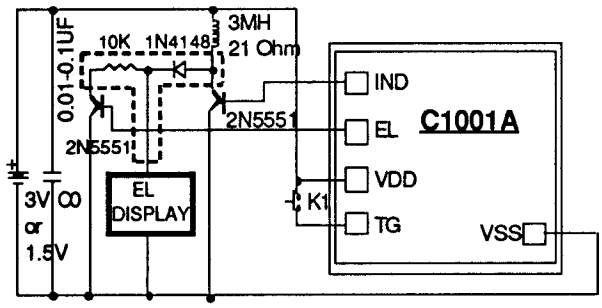


B. Application with 3 Second Delay using Vss Trigger & without Delay using FLSH Trigger

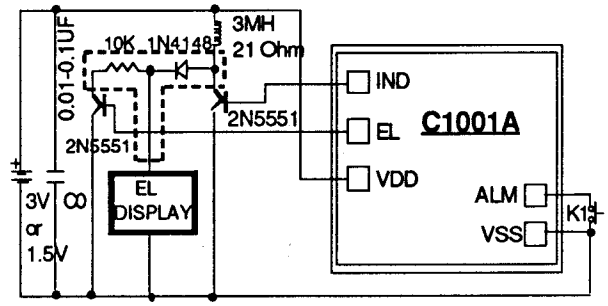


NOTE: Substrate is connecter to VDD

C. Application with 3 Second Delay using Vdd Trigger

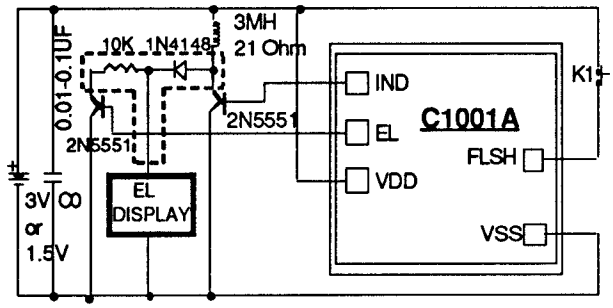


D. Application with 3 Second Delay using Vss Trigger

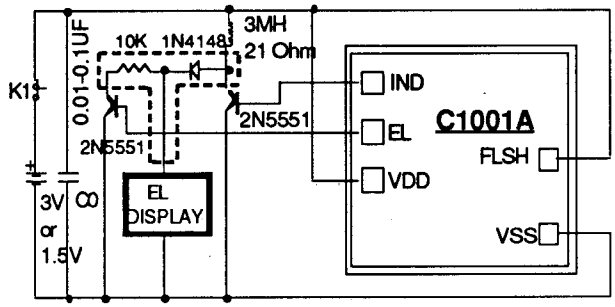


NOTE: Substrate is connecter to VDD

E. Application without Delay using FLSH Trigger



F. Application without Delay using Power Button



NOTE: Substrate is connecter to VDD

NOTE: 1. Substrate is connecter to VDD
2. L* and R* are adjustable to enlarge the driving capability.