Specification for C9005
(custom design counter chip)

date : 16 May 1991 / version 03

General Description

C9005 is an up-graded version of C9003. It applies the technology of 2μm Polysilicon gate P well CMOS which enable small dies size and low power dissipation.

3 sets of counters (R6, R3, and R4) are implemented which can be operated simultaneously.

Important features of C9005 are listed in below :

* 1.35 to 1.7 Volt operating range.
* built in Quartz oscillator required 32768 Hz quartz crystal and 8 - 20 pF trimming capacitor as external components.
* full 4 digits LCD include 3 display-mode flags and 1 decimal point.
* DMS button for Display-mode select.
* 3 digits counter constant setable by user.
* SW button to select digit to set constant.
* SS button to increment digit during set constant.
* Schmitt triggered input IN1 for PI pulses input.
* internal 3.6 msec time pulse generator.
* auto power-up reset.
* single button reset for R3 counter.

Functional description

The device provides 3 sets of counters, R6, R3, and R4 .

(1) R6 counter - R6 counting is a division of R1 by N. Register R1 held a 3 digits constant set by user, and register N counts the number of 3.6 msec time pulses encountered between 2 consecutive PI pulses.

(2) R3 & R4 counters - Both R3 and R4 count the number of SCF pulses. For every PI, the content of R1 is accumulated in register R2 and SCF pulse is generated whenever R2 overflows . R3 is a 4 digits counter resetable by RS button while R4 is a 5 digits counter reset only at power up.

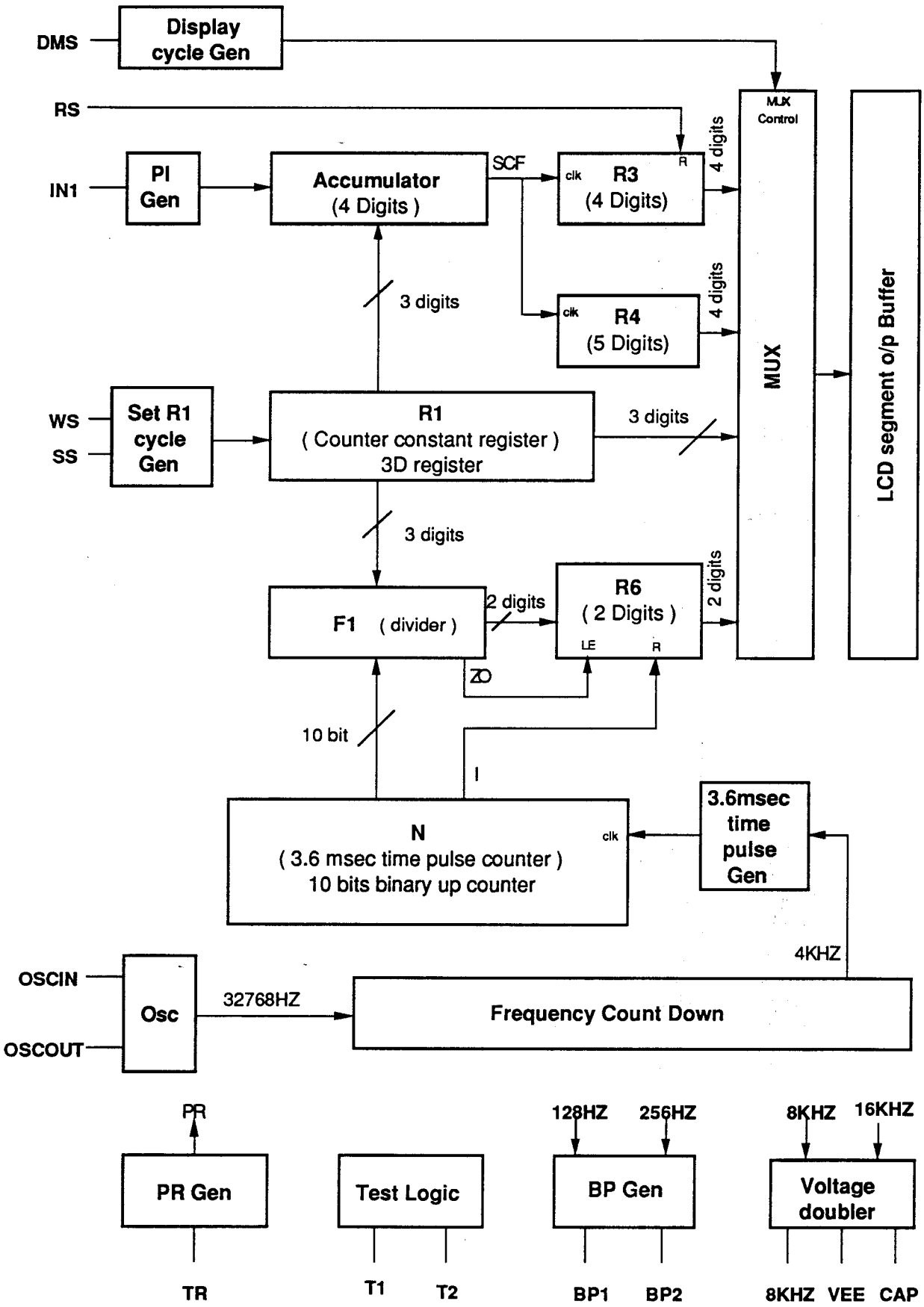
3 display modes corresponding to these counters are provided. DR6 is the initial mode followed by DR3 and DR4. They can be selected in sequential order by button DMS. Whenever set counter constant cycle active (Set R1 active), the content of R1 is displayed (DR1) and DR6 will be resumed upon exited.

Functional blocks

1. Oscillator

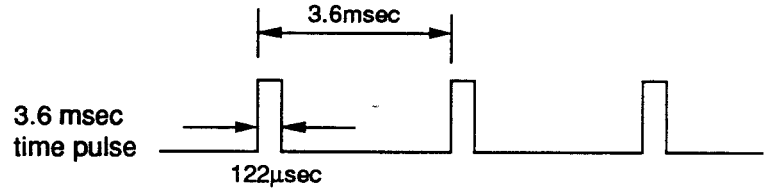
A 32768 Hz quartz oscillator is implemented to generate the system clock. The clock is binary countdown to provide internal circuit controls. The 3.6 msec time pulses are generated from the 4 kHz clock which is one of the outputs from the binary countdown .

Functional Block Diagram



2. 3.6 msec time pulse generator

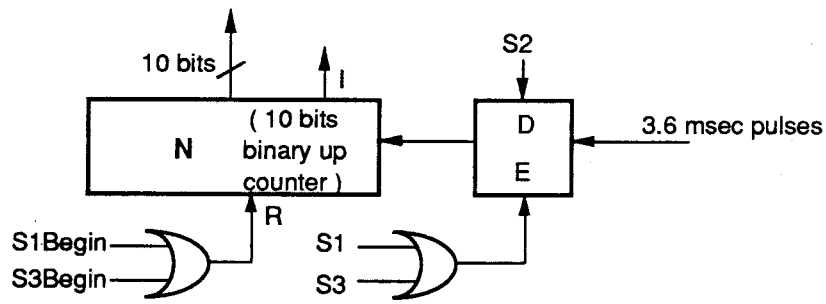
Pulses of width 122 μsec and period 3.6 msec is generated from a 4 stages counter with the input clock equal to 4 kHz, a tolerance of less than 2% is expected.



3. 3.6 msec time pulse counter (N)

N is a 10 bits binary up counter which will be reset at the beginning of logic stages S1 and S3 of division cycle. It will count during S1 and S3 the number of 3.6 msec time pulses encountered .

Signal I will be generated when N overflows. Counter R6 will be reset; and if it happens in S1 stage, S1 will be switched to S3 by I.



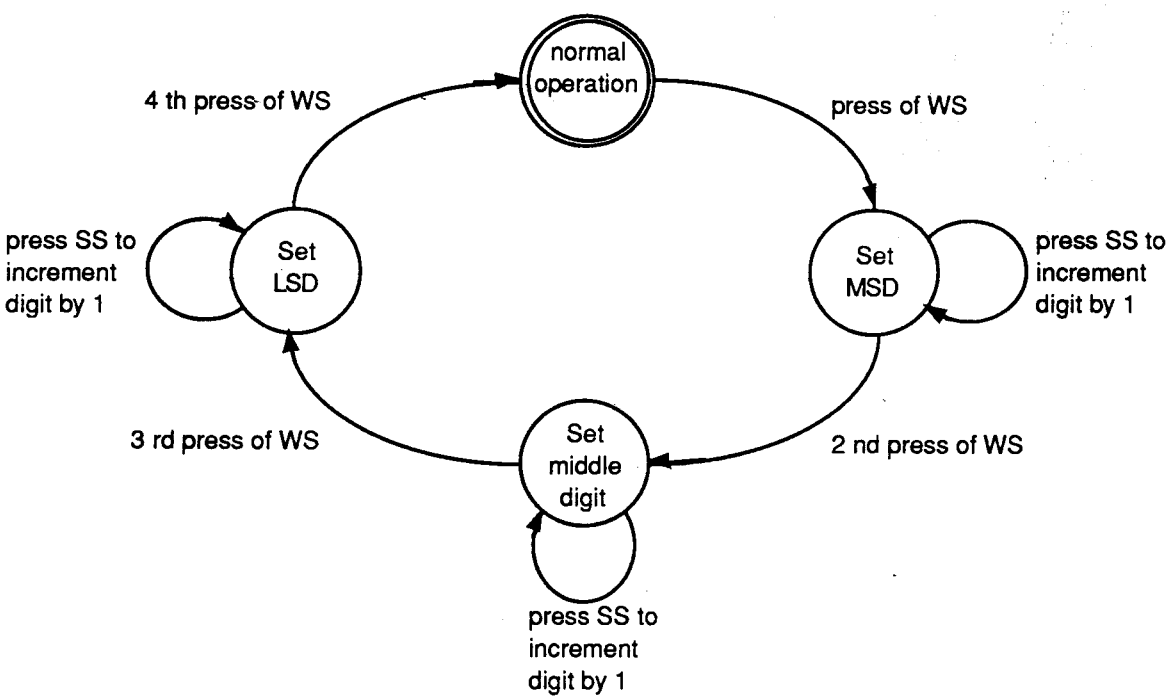
4. Pulse input (PI generator)

It is a Schmitt triggered input for external input PI pulses. The minimum time interval between 2 consecutive pulses must be larger or equal to 70 msec.

No internal pull down nor debounce is provided for this input, and it will not accept input when the Set R1 cycle is active.

5. Set R1 cycle generator

The Set R1 cycle is activated by WS button.



Upon the 1 st press of WS, the counter constant (content of R1)will be displayed on the right most 3 digits of the LCD panel with the most significant digit flashing once every second. The flashing digit will increment by 1 for each press and release of SS.

Upon the 2 nd press of WS, the 2 nd digit from the right will flash, increment of digit same as before.

Upon the 3 rd press of WS, the right most digit will flash, increment of digit same as before.

Upon the 4 th press of WS, the Set R1 cycle is exited, normal operation is resumed with the display mode cycle reset to DR6, and the division cycle reset to S3.

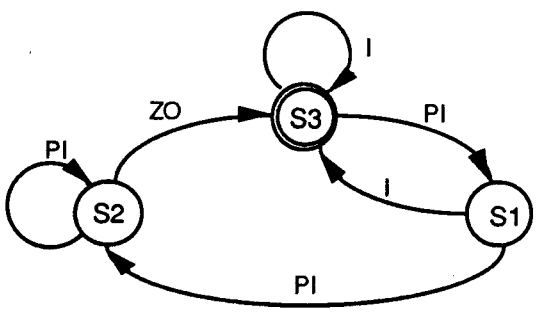
6. Counter constant register (R1)

R1 is a 3 digits register for memorizing the counter constant defined by user with buttons WS and SS. Internal pulldown and 32 Hz debounce are provided for these 2 inputs.

When Set R1 cycle is activated : display cycle is switched to DR1, all counting operations are stopped, all internal state machines are reset to their initial states, inputs such as PI and DMS will be ignored except WS AND SS.

7. Division cycle generator

A division cycle state machine is implemented to control the operations of the counters involved. It consists of 3 logic states : the initial state S3, 3.6 msec time pulse counting state S1, and the division state S2.



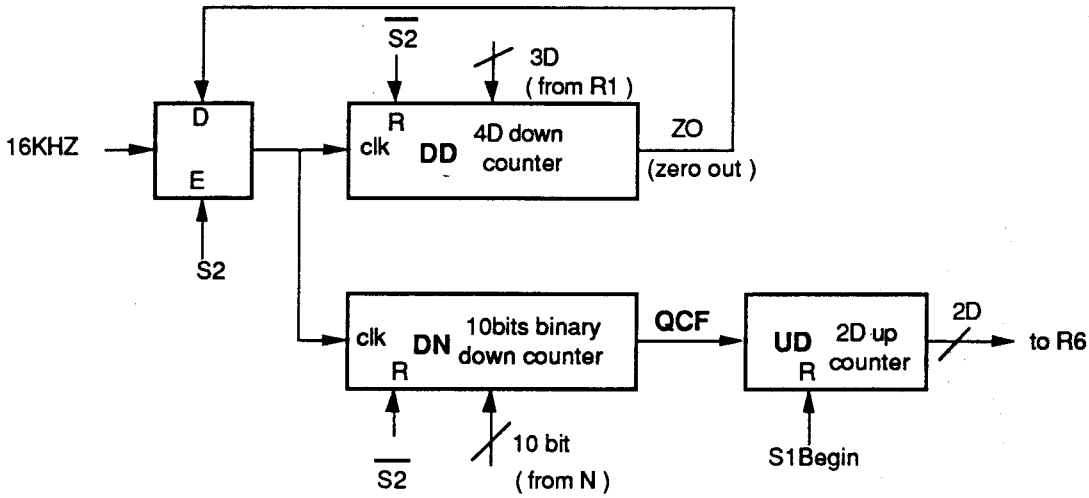
At S3, the time pulse counter N is reset and counts. Overflow signal I is generated when N counts full. S3 is maintained until PI is detected which switches the division cycle to S1.

At S1, counter N is reset and start counting the 3.6 msec time pulses until the next PI detected. S1 is then switched to S2 for division to take place. When I occurs before or at the same time as PI, the division cycle will be switched to S3 instead.

At S2, division takes place and PI will be ignored. S2 switches back to S3 by ZO.

8. Divider (F1)

The dividend equals to R1 multiplied by ten, and the divisor equals to N. Division takes place at S2 when N stops counting. Its content (divisor)



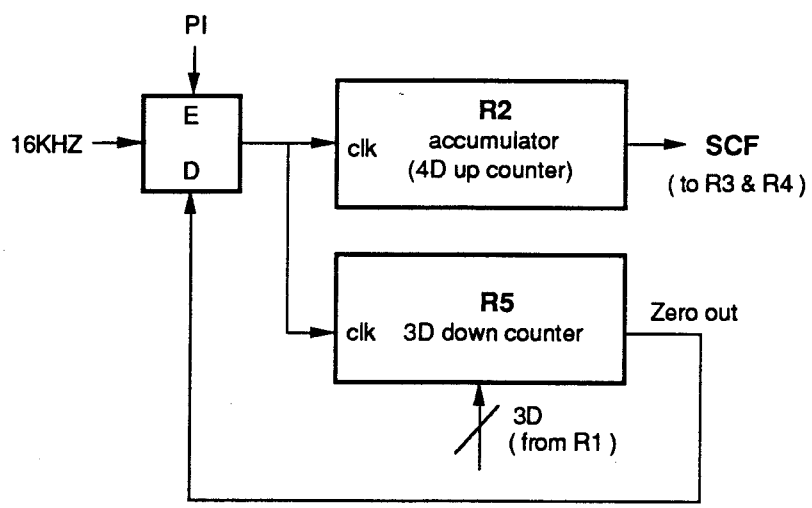
is loaded to a 10 bits binary down counter DN when R1 (dividend) is loaded to the left most 3 digits of a 4 digits BCD down counter DD, the least digit being set to zero. A common clock of 16 kHz is applied to the 2 counters and a 2 digits BCD up counter UD is increment 1 each time DN zero out. DN is reloaded and the process repeats until DD is zero out. Signal ZO is thus generated and the content of UD is the integer value of the quotient which will be load to R6 for display. S2 is switched to S3 by ZO.

R6 is a 2 digits latch for temporary storage of output from UD. LE input of R6 is essentially controlled by ZO and a 2 Hz square wave such that data loading from UD will not be faster than twice a second.

UD is reset at the beginning of S1, R6 is reset whenever I becomes active; DN and DD are forced zero except in S2. And they all reset by Set R1.

9. Counter constant accumulator (R2)

R2 is a 4 digits BCD up counter which will increment by the amount of the counter constant on each PI. The addition is done by loading the counter constant to a 3 digits down counter R5, and both R2 and R5 is clocked by a 16 kHz signal until R5 zero out when the accumulation accomplished. SCF signal is generated when R2 overflow, which will output to register R3 and R4 for counting. Set R1 signal will reset R2 and R5.

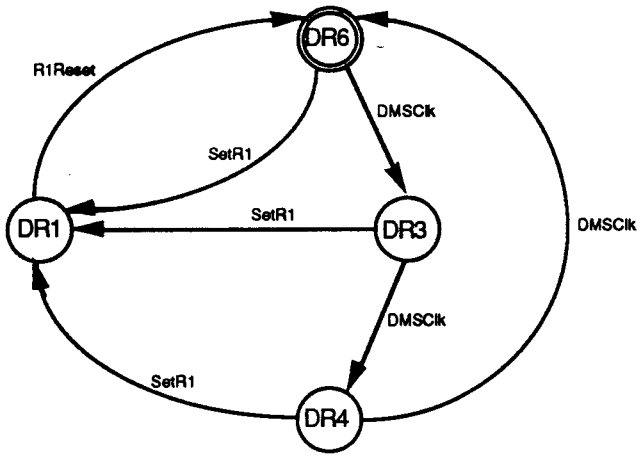


10. SCF Counters (R3, R4)

R3 is a 4 digits counter and R4 is a 5 digit counter. They both count the number of SCF pulses encountered. R3 can be reset by external input signal RS whereas R4 is reset only at power up. Internal pulldown and 32 Hz debounce is provided for RS.

11. Display cycle generator

The data flow from internal counters to LCD display is controlled by the display cycle generator. The initial state at power up is DR6, with every press on DMS button it will cycle through DR3, DR4 and then back to DR6 again.



In DR6, R6 is displayed on the right 2 digits with the left 2 digits blanked. In DR3, R3 is displayed with a decimal point between the 1 st and the 2 nd digits from the right, blank leading zero of up to 2 digits is provided. In DR4, the least 4 digits of R4 is displayed without blank leading zero. Three display mode flags indicating mode status are provided.

Display will be switched to DR1 whenever Set R1 cycle active no matter which is previously on. DR6 will be resumed after Set R1 cycle is exited.

Internal pulldown and 32 Hz debounce is provided for DMS input.

12. PR generator

In normal condition, reset pulse PR is generated at power up to reset all internal logic. All counters/registers will be reset except R1 which holds the customer input constant. PR signal can be generated through the TR pad for test purpose.

Test inputs

1. TR

External reset signal can be input through TR pad to generated a PR signal at any time.

2. T1

This is a test input for testing LCD display pattern. When T1 is active, all display mode flags, decimal point and LCD segments are ON enable user to find any segment malfunction. No reset action will be caused by T1.

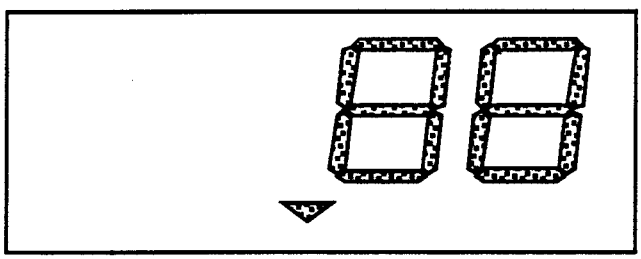
3. T2

This is a test input to speed up counting. When T2 is active, all counters (R6, R3 and R4) will count in the manner of 1111, 2222, 3333 and so forth. This enable a 4 digits BCD counter counts from 0000 to 9999 in 9 clock pulses.

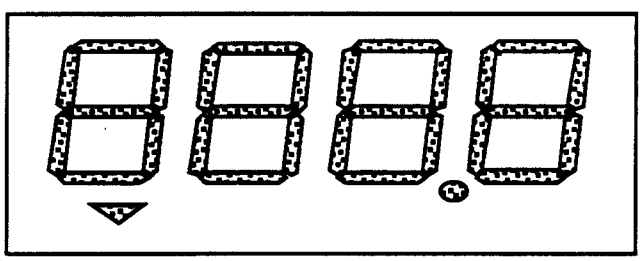
LCD component

Biplex, full 4 digits Liquid crystal display panel with a decimal and 3 display mode flags will be used for this device

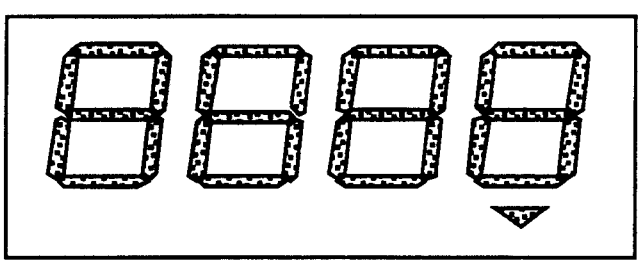
Display Pattern under different display modes



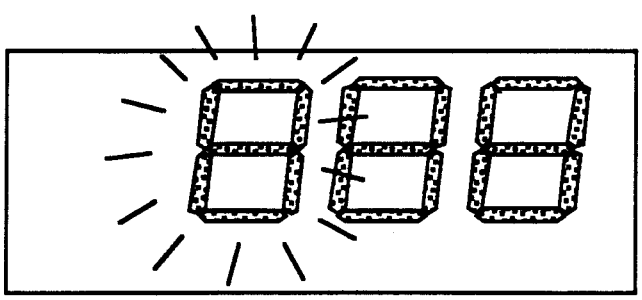
Display mode DR6
2 digits of R6 are displayed on the right with the 2 leading digits blanked.
A flag in the middle is displayed.



Display mode DR3
the 4 digits of R3 are displayed with blank leading zero of up to 2 digits.
A flag and a decimal are displayed.



Display mode DR4
the left most 4 digits of R4 are displayed. No leading zero blanking is provided.
A flag on the right is displayed.



Set R1 period
the counter constant is displayed on the right 3 digits with the selected digit blinking.

List of pads

Vdd, Vss	+ve and ground supply pads.
OSCIN	32768 Hz Quartz oscillator's input.
OSCOUT	32768 Hz Quartz oscillator's output.
PI	PI pulse input, with Schmitt triggered input.
DMS	display mode select, with internal pulldown and 32 Hz debounced.
WS	set counter constant digit select, with internal pulldown and 32 Hz debounced.
SS	digit increment for set counter constant, with internal pulldown and 32 Hz debounced.
RS	reset input for R3 register, internal pulldown and 32 Hz debounced.
TR	master reset input.
T1	LCD test input, with internal pulldown.
T2	BCD counter test input, with internal pulldown.
8 kHz	8 kHz clock output for voltage doubling.
CAP	connection pad for voltage doubler capacitor.
VEE	voltage doubled output.
BP1, BP2	backplane signals output.
F1/E1	segment output.
A1/G1	segment output.
B1/C1	segment output.
DR4 FLAG/D1	segment output.
F2/E2	segment output.
A2/G2	segment output.
B2/C2	segment output.
/D2	segment output.
F3/E3	segment output.
A3/G3	segment output.
B3/C3	segment output.
DR3 FLAG/D3	segment output.
F4/E4	segment output.
A4/G4	segment output.
B4/C4	segment output.
DR6 FLAG/D4	segment output.

total of 33 pads.

Parameters

1. **Specification of input**
   a. The minimum time interval between 2 consecutive PI pulses is 70 msec, error in registers R2 and R6 may occur if it is violated.

   b. The maximum value of user input counter constant is 400, any value larger than this is not allowed, and may cause error in registers R2 and R6.

   The maximum addition time for R2 is less than 25 msec according to (b), well before next PI arrives according to (a). The maximum division time for F1 can be as long as 245 msec according to (b), PI will be ignored by the Division cycle generator until division is over.

2. Absolute maximum ratings

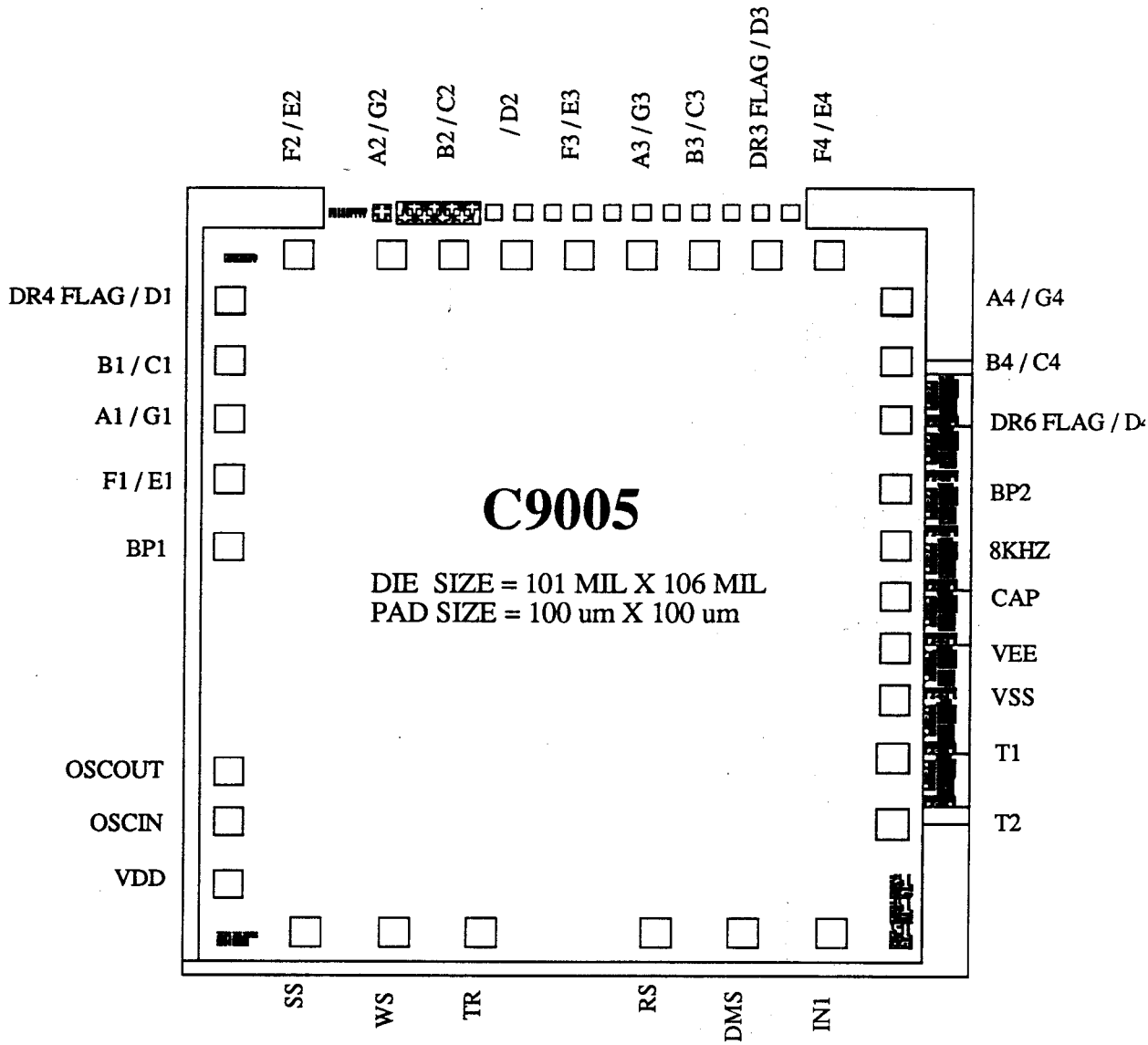
Parameter	Range	Unit
Storage temperature	- 50 to + 150	C
Operating temperature	0 to + 50	C
Supply voltage : Vdd - Vss Vdd - Vee	2 4	Volt Volt
Input voltage range	Vss < Vin < Vdd	
Output voltage range	Vss < Vout < Vdd	
LCD output range	Vee < Vout < Vdd	

3. Electrical parameters

Vdd = 1.5 Volt
Vss = 0.0 Volt
TA = 25 C
(Voltage doubler connected unless otherwise specified.)

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage (Vdd)		1.35		1.7	Volt
Supply current (Idd)	LCD disconnected		8.0	13.0	µA
Doubler output voltage	I_H = 1.0 µA		- 1.3		Volt
Segment ON voltage	Vee =- 1.3 V (rms)		2.27		Volt
Segment OFF voltage	Vee =- 1.3 V (rms)		1.06		Volt
Power consumption				0.02	mW

C9005 \ PAD DIAGRAM

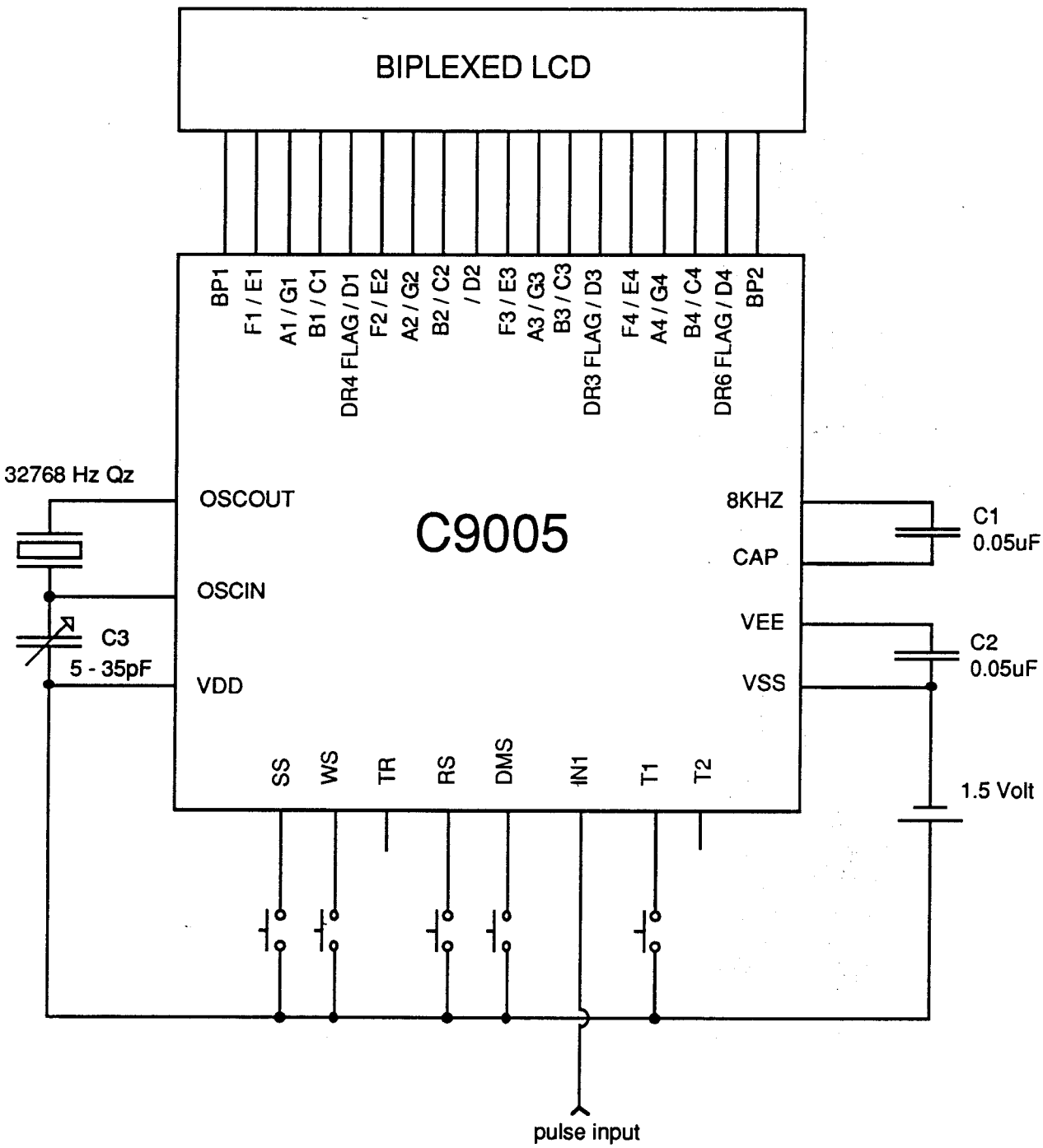


PAD CENTER COORDINATES

(values reflect true dimensions on wafer with origin at dies center)

BP1	(-1121, 160)	BP2	(1121, 372)
F1 / E1	(-1121, 392)	8KHZ	(1121, 168)
A1 / G1	(-1121, 602)	CAP	(1121, -11)
B1 / C1	(-1121, 813)	VEE	(1121, -191)
DR4 FLAG / D1	(-1121, 1023)	VSS	(1121, -372)
F2 / E2	(-888, 1191)	T1	(1121, -569)
A2 / G2	(-579, 1191)	T2	(1121, -806)
B3 / C3	(-368, 1191)	IN1	(915, -1191)
/ D2	(-158, 1191)	DMS	(619, -1191)
F3 / E3	(52, 1191)	RS	(323, -1191)
A3 / G3	(263, 1191)	TR	(-265, -1191)
B3 / C3	(473, 1191)	WS	(-561, -1191)
DR3 FLAG / D3	(684, 1191)	SS	(-856, -1191)
F4 /E4	(895, 1191)	VDD	(-1121, -1026)
A4 / G4	(1121, 1023)	0SCIN	(-1121, -805)
B4 / C4	(1121, 813)	OSCOUT	(-1121, -625)
DR6 FLAG / D4	(1121, 602)		

C9005 APPLICATION DIAGRAM



TR - option input for testing, connect it to VSS will force the device to power-up reset.
T2 - option input for testing.