RCL Semiconductors Ltd.

Custom Design Counter Device C9006

General Description

C9006 is a custom designed counter device using our 1.8um N well Poly Gate CMOS technology which enables small die size and low power dissipation. 3 sets of counters are provided which can be operated simultaneously. The display-mode select function is used to select which of the 3 counters to be displayed on LCD.

Features

* 1.35 to 1.7 Volt operating range.
* Built-in Quartz Oscillator required 32768Hz quartz crystal and 8-20 PF trimming capacitor as external components.
* Full 4 digits LCD including 3 display-mode flags and 1 decimal point.
* 3 digits counter constant(R1) and 6 digits counter register(R4) are settable by user.
* WS button controls access of R1 setting and exit of R1& R4 setting.
* DMS button for digit selection during R1&R4 setting and display-mode selection in normal operation.
* RS button for digits increment during R1&R4 setting, also for reset of R3 counting by RS pressed continuously for 2 second.
* Schmitt triggered input IN1 to sense input pulses. R2 adds the value of R1 whenever a pulse comes in from IN1. R3 and R4 increments by 1 when R2 is overflow.
* Internal 3.6 ms pulse generator used as sample clock.
* Auto power-up reset and keep all LCD segments lighting for 1 second while power up reset. Clear all registers after power-up reset and the initial value for R1 is 216, whereas for R4 is zero(0000) and R4 is set only at setting mode.

Functional Description

The device provides 3 sets of counters: R6, R3 and R4 .

1. R6 counting - R6 counting is a division of R1 by N (R6=10R1/N).
   1.1. Register R1 is used to memorize a 3 digits counter constant which can be set by user using button DMS and RS. The access and exit of R1 setting is controlled by WS button.
   1.1.1. When WS pressed continuously for 0.5 second during normal operation, the content of R1 will be displayed on the right most 3 digits of LCD panel, with the most significant digit blinking twice a second, and the blinking digit will increment by 1 whenever RS button pressed once.
   1.1.2. The 2nd digit from right will blink when DMS button pressed at the 1th time, and the blinking digit will increment by 1 whenever RS button pressed once.
   1.1.3. The similar procedure for setting the right most blinking digit when DMS button pressed at the 2nd time.
   1.1.4. The most significant digit will blink again when DMS pressed at the 3rd time to begin another cycle, so and so on.....
   1.1.5. During above setting process, C9006 will exit the procedure by WS button pressed once and return to the display mode which is the one before access R1 setting.
   1.2. Register N is used to count the number of 3.6 msec time pulse encountered between 2 consecutive PI pulses.

2. R3 & R4 counting - Both R3 and R4 count the number of SCF pulses generated from R2 (Counter Constant Accumulator). For every PI, the content of R1 is added to register R2 and SCF signal is generated when R2 overflows .
   2.1. R3 is a 5 digits counter resetable by RS button pressed continuously for 2 second.

2.2. R4 is a 6 digits counter reset only at power up. But only the most 4 digits can be displayed on LCD.. Only after power-up reset, R4 can be set by user. The setting procedure to display 4 digits value of R4 register is as same as R1 setting. During any digit setting for R4 counter register, as long as WS button is pressed once, it will exit the setting procedure and DR4 should display. Furthermore, it cann't re-entry setting mode for R4 register after exiting R4 setting by pressing WS once, except power-up reset again.

The device provides 3 display modes corresponding to the three counters. In normal operation(i.e. exit from R4 setting), DR4 is the initial display mode followed by DR3, DR6 and then back to DR4. The display mode changes once in this sequence by pressing DMS button once.

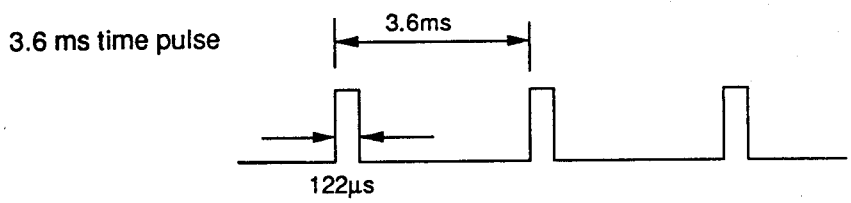
Functional Blocks

1. Oscillator

A 32768Hz quartz oscillator is implemented as the clock generator. The 32768 Hz clock is output to a binary countdown from which a number of divided signals are generated for internal circuit controls. The 3.6 msec time pulses are generated from the 4kHz clock which is also one of the outputs from the binary countdown .

2. 3.6 msec time pulse generator

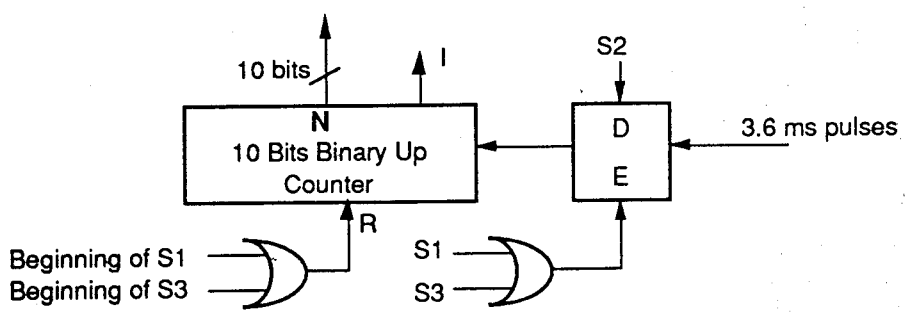
Pulses of width 122 µs and period 3.6 ms is generated from a 4 stages counter with the input clock equal to 4kHz, a tolerance of less than 2% is expected.



3. 3.6 msec time pulse counter (N)

N is a 10 bits binary up counter which will be reset at the beginning of logic stages S1 and S3 of division cycle. During S1 and S3, it will count the number of 3.6 ms time pulses encountered .

Signal I will be generated to reset counter R6 when N overflows. And if it happens in S1 stage, S1 will be switched to S3 by I.



4. Pulse input (PI generator)

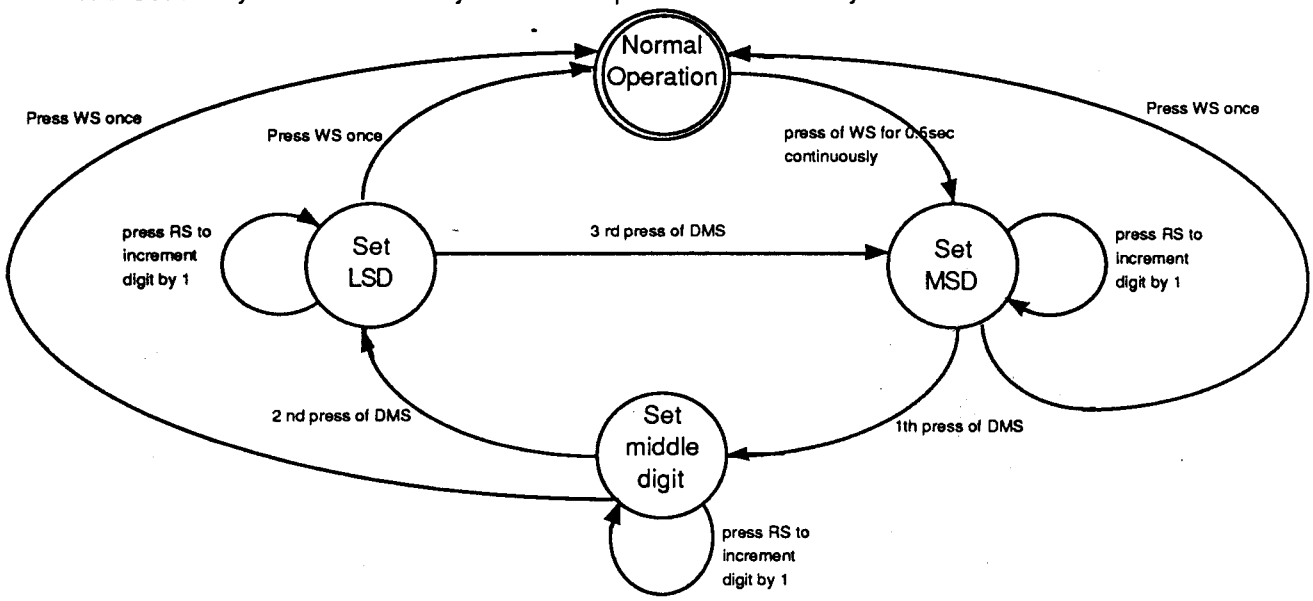
A Schmitt triggered input circuit is implemented to sense the external PI pulses. The minimum time interval between 2 consecutive pulses must be equal or larger than 70 msec. Internal pull down resister 50K(24K to 72K) is provided for this input (IN1). It will not accept input PI pulses when setting R1 Counter Constant Register and R4 Counter.

5. Counter constant register (R1)

R1 is a 3 digits register assigned for memorizing the counter constant which can be defined by user with buttons WS, DMS and RS. Internal pulldown and 32 Hz debounce are provided for the 3 inputs WS, DMS and RS. When Set R1 Cycle is activated: display cycle is switched to DR1, all counting operations are stopped, all internal state machines are reset to their initial states, input IN1 will be ignored.

6. Set R1 cycle generator

The Set R1 cycle is activated by WS button pressed continuously for 0.5 second.



At the normal operation, upon the press WS for 0.5sec continuously, the counter constant (content of R1)will be displayed on the right most 3 digits of the LCD panel with the most significant digit blinking twice every second. The blinking digit MSD will increment by 1 for each press of RS button.

Upon the 1th press of DMS, the 2nd digit from the right will blink and press of RS button will increment the middle digit as above.

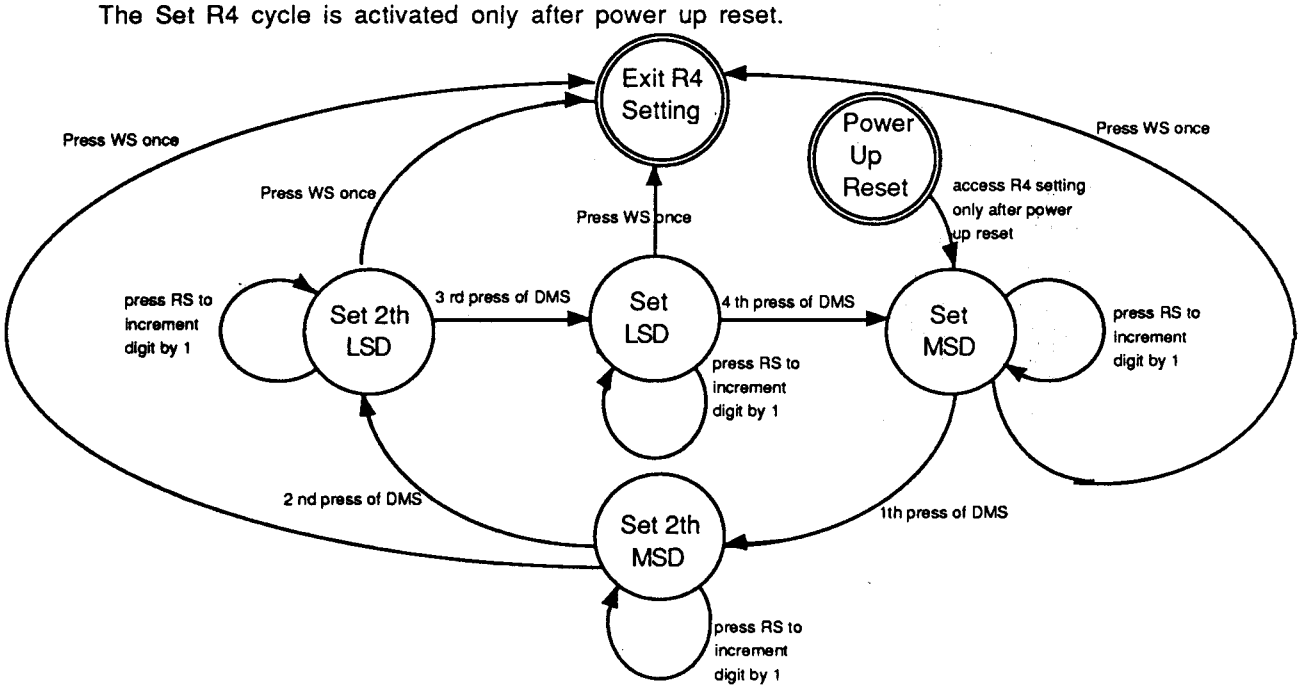
Upon the 2nd press of DMS, the right most digit will blink and press of RS button will increment the digit LSD as above.

Upon the 3rd press of DMS, it will cycle back to the most significant digit blinking, increment of digit as same as above.

During setting process for MSD, middle digit and LSD, whenever pressing WS once, it will exit setting and return to the normal operation mode which is the one before access R1 register setting.

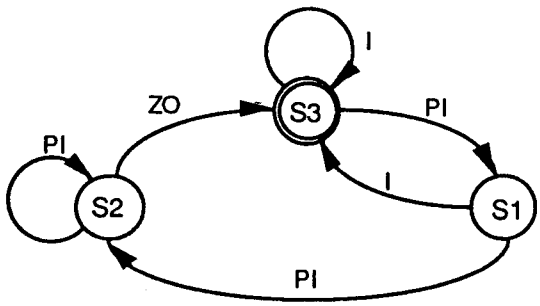
7. Set R4 cycle generator

The Set R4 cycle is activated only after power up reset.



After power up reset, C9006 can automatically access R4 setting. The setting procedure is as same as R1. It will exit R4 setting by pressing WS once during the setting for any digit of R4 and can not access R4 setting again, except power up reset.

8. Division cycle generator



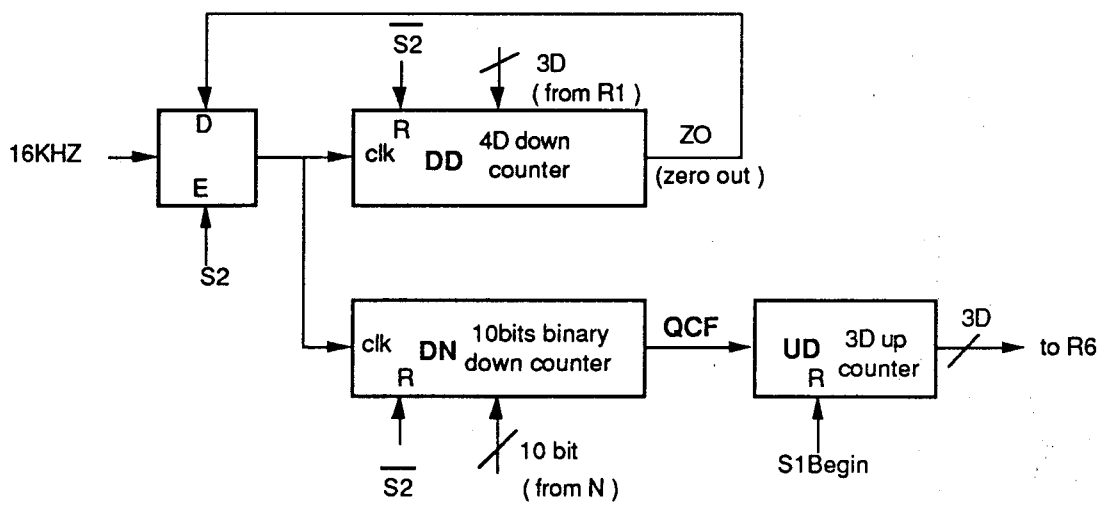
A division cycle is implemented to control the operations of the counters involved. It consists of 3 logic states : the initial state S3, 3.6ms time pulse counting state S1, and the division state S2.

At S3, the time pulse counter N is reset and counts. Overflow signal I is generated when N counts full. S3 is maintained until PI is detected which switches the division cycle to S1.

At S1, counter N is reset and start counting the 3.6 msec time pulses until the next PI detected. S1 is then switched to S2 for division to take place. When I occurs before or at the same time as PI, the division cycle will be switched to S3 instead.

At S2, division takes place and PI will be ignored. S2 switches back to S3 by ZO.

9. Divider (F1)



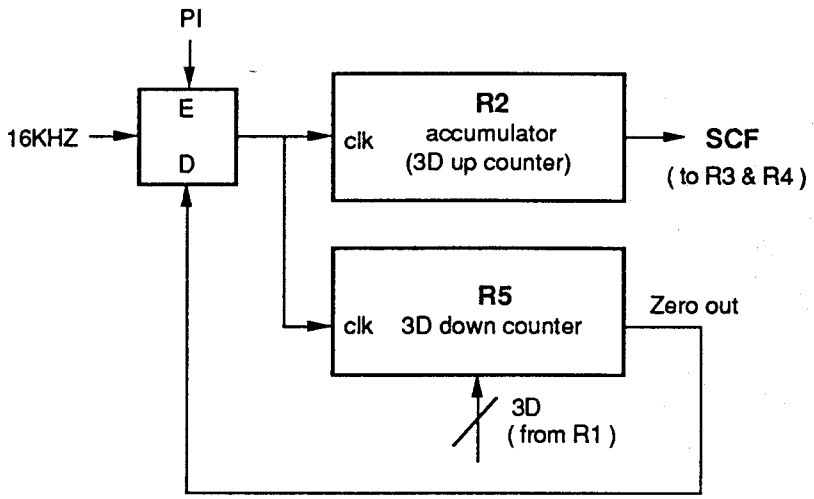
The dividend equals to R1 multiplied by ten, and the divisor equals to N. Division takes place at S2 when N stops counting. Its content(divisor) is loaded to a 10 bits binary down counter DN when R1(dividend) is loaded to the left most 3 digits of a 4 digits BCD down counter DD, the least digit being set to zero. A common clock of 16kHz is applied to the 2 counters and a 3 digits BCD up counter UD is increment 1 each time DN zero out. DN is reloaded and the process repeats until DD is zero out. Signal ZO is thus generated and the content of UD is the integer value of the quotient which will be load to R6 for display. S2 is switched to S3 by ZO.

R6 is a 3 digits latch for temporary storage of output from UD. LE input of R6 is essentially controlled by ZO and a 2 Hz square wave such that data loading from UD will not be faster than twice a second.

UD is reset at the beginning of S1, R6 is reset whenever I becomes active; DN and DD are forced zero except in S2. And they all reset by Set R1.

10. Counter constant accumulator (R2)

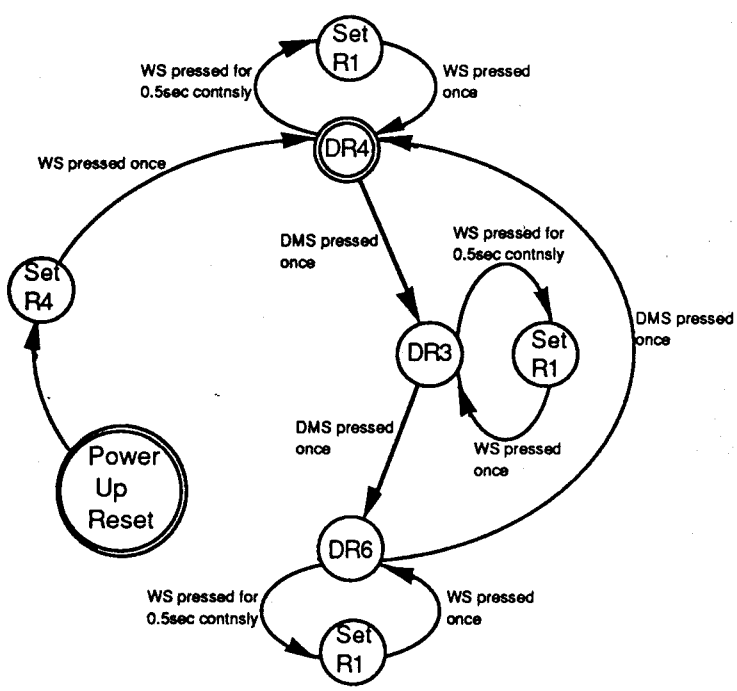
R2 is a 3 digits BCD up counter which will increment by the amount of the counter constant on each PI from IN1. The addition is done by loading the counter constant to a 3 digits down counter R5, and both R2 and R5 is clocked by a 16kHz signal until R5 zero out when the addition is accomplished. SCF signal is generated when R2 becomes overflow, which will output to register R3 and R4 for counting. Set R1 signal will reset R2 and R5.



11. SCF Counters

R3 is a 5 digits counter and R4 is a 6 digits counter. They both count the number of SCF pulses encountered. R3 can be reset by external input signal RS, whereas R4 is reset only by power up. Internal pulldown and 32Hz debounce is provided for RS.

12. Display cycle generator



Display cycle control the data flow from internal counters to LCD display. After power up, it can automatically access R4 setting, but it will exit R4 setting by WS pressed once and followed by the normal operation mode DR4, with every press on DMS button it will cycle through DR3, DR6 and then back to DR4 again. It will be unable to access R4 setting again after exit R4 register setting except power up reset again

However, it can access R1 setting by WS pressed continuously for 0.5 second during any one of the normal operation mode. Furthermore, it will exit R1 setting by WS pressed once and return to the display mode which is the same one before access R1 setting.

In DR4, the left most 4 digits of R4 is displayed without leading zero blanked.

In DR3, R3 is displayed with a decimal point between the 1st and the 2nd digits from the right. Blanked leading zero of up to 2 digits is provided.

In DR6, R6 is displayed on the right most 3 digits with the left most digit blanked.

Display mode flags indicating each mode status can be seen on the LCD panel.

Internal pulldown and 32 Hz debounce is provided for DMS input.

13. PR generator

In normal condition, reset pulse PR is generated at power up to reset all internal logic. In additions, external reset signal can be forced through the TR pad to generated a PR signal at any time.

Test Inputs

1. TR

External reset signal can be input through TR pad to generated a PR signal at any time. The whole device will be reset.

2. T0

An external clock signal can be forced through T0 into the divider chain of the OSC(refers to the "Frequency Counter Down" in "Functional Block Diagram") to speed up the testing. During test mode, T0 is connected to f_{32} point at which the OSC frequency has divided by 32.

3. TDS

This is a test input for testing LCD display pattern. When TDS is active, all display mode flags, decimal point and LCD segments are ON enable user to find any segment malfunction. No reset action will be cause by TDS.

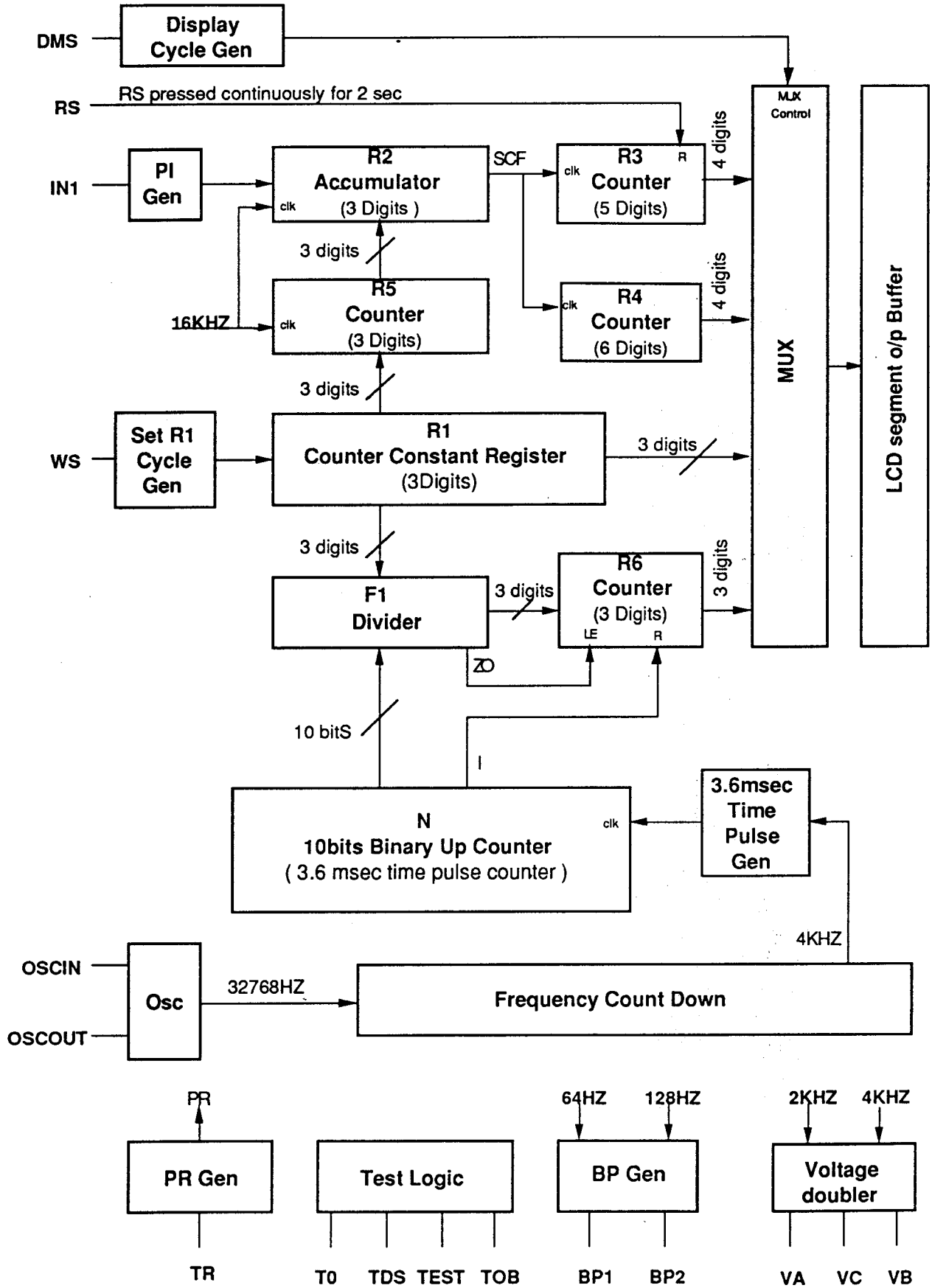
4. TEST

This is a test input to speed up counting. When TEST is active, all BCD counters (no matter up counting or down counting) will count in the manner of 1111, 2222, 3333 and so forth. This enable a 4 digits BCD counter counts from 0000 to 9999 in 9 clock pulses.

5. TOB

This is a test input for observation of 3.6ms pulses and flags on LCD display.

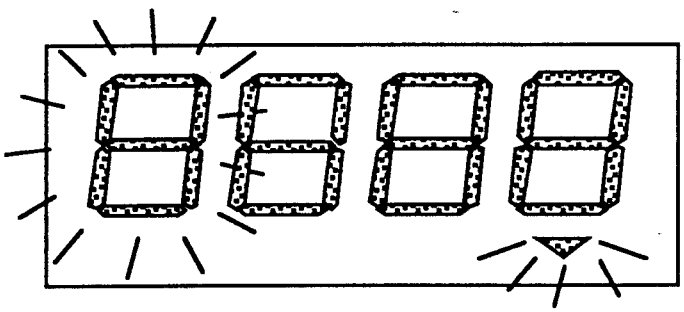
Functional Block Diagram



LCD Component

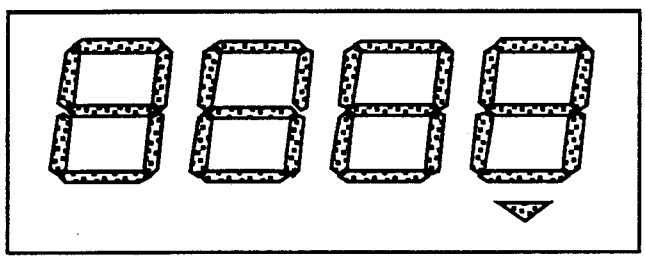
Biplex, full 4 digits Liquid Crystal display panel with a decimal and 3 display mode flags will be used for this device. The LCD drive frequency is 64Hz.

Display Pattern Under Different Display Modes



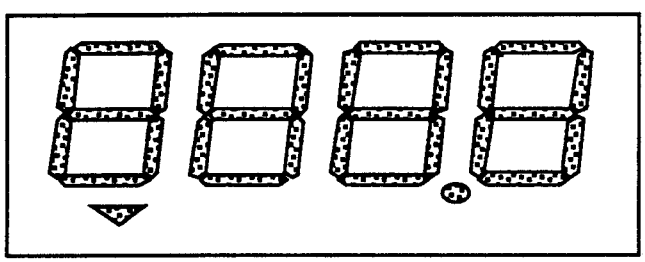
Set R4 Period

the digit value for the left most 4 digits of R4 can be set after power up, with the selected setting digit blinking.
A mode flag should be blinking during R4 setting.



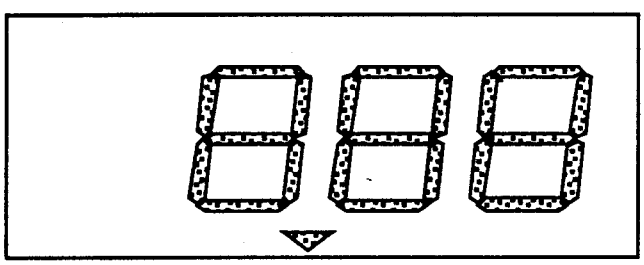
Display Mode DR4

the left most 4 digits of R4 are displayed.
No leading zero blanked is provided.
A flag on the right is displayed.



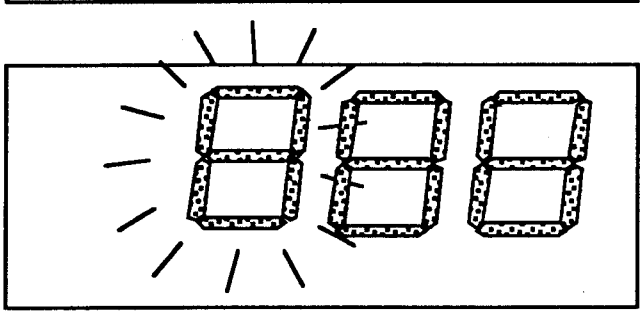
Display Mode DR3

the left most 4 digits of R3 are displayed with leading zero blanked of up to 2 digits.
A flag and a decimal are displayed.



Display Mode DR6

the 3 digits of R6 are displayed on the right with the leading digit blanked up to 2 digits.
A flag in the middle is displayed.



Set R1 period

the counter constant is displayed on the right 3 digits with the selected digit blinking.
No flag is displayed.

List Of Pads

Vdd, Vss	Power and ground supply pads.
OSCIN	32768Hz Quartz oscillator's input.
OSCOUT	32768Hz Quartz oscillator's output.
IN1	Pulse input, with Schmitt triggered input and 50K pulldown resistor.
DMS	Display mode selection, with internal pulldown and 32Hz debounced.
WS	Set counter constant digit selection, with internal pulldown and 32Hz debounced.
RS	Reset input for R3 register, internal pulldown and 32Hz debounced.
TR	Master reset input.
TO	Test input. An external clock signal can be forced through TO into the divider chain of OSC to speed up testing.
TOB	Test obserbility for control signal of LCD and clock of 3.6 ms counter.
TDS	LCD test input, with internal pulldown.
TEST	BCD counter test input, with internal pulldown.
VA	2KHz clock output for voltage doubling.
VB	Connection pad for voltage doubler capacitor.
VC	Voltage doubled output.
BP1, BP2	Backplane signals output.
F1/E1	Segment output.
A1/G1	Segment output.
B1/C1	Segment output.
DR4 FLAG/D1	Segment output.
F2/E2	Segment output.
A2/G2	Segment output.
B2/C2	Segment output.
/D2	Segment output.
F3/E3	Segment output.
A3/G3	Segment output.
B3/C3	Segment output.
DR3 FLAG/D3	Segment output.
F4/E4	Segment output.
A4/G4	Segment output.
B4/C4	Segment output.
DR6 FLAG/D4	Segment output.

total of 34 pads.

Parameters

1. Specification of input

1.1. The minimum time interval between 2 consecutive PI pulses from IN1 input is 70 msec, error in registers R2 and R6 may occur if it is violated. The width of PI pulses is 100us to 1s, the rising and falling edge of PI pulses is 50us to 200ms. The internal pull down resister 50K(24K to 72K) and an external debounce circuit (delay 15 ms from the rising edge) is provided for IN1.

1.2. The value of user input counter constant (R1) is from 000 to 999. But error in registers R2 and R6 are acceptable when the value of R1 is larger than 400.

The maximum addition time for R2 is less than 25 msec according to 1.2, well before next PI arrives according to 1.1. The maximum division time for F1 can be as long as 245 msec according to 1.2, PI will be ignored by the Division cycle generator until division is over.

2. Absolute maximum ratings

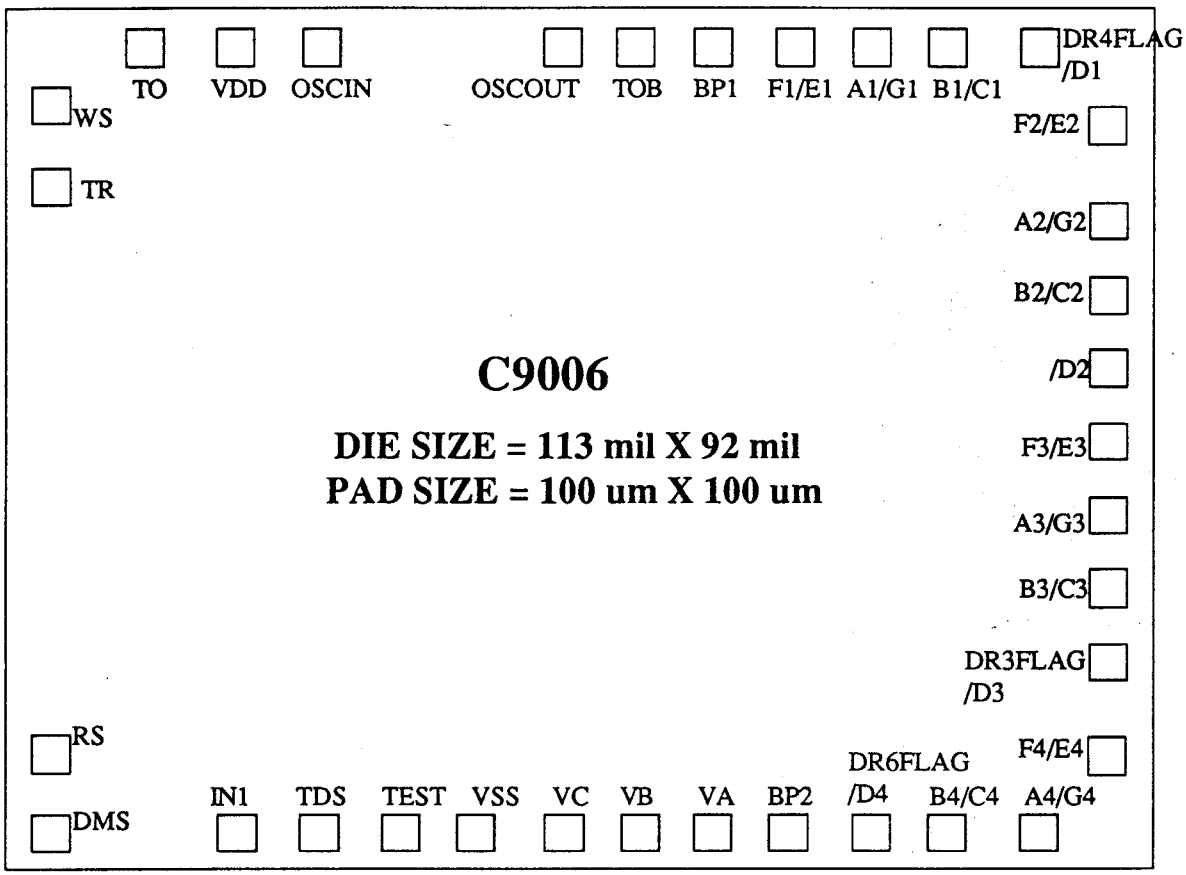
Parameter	Range	Unit
Storage temperature	- 50 to + 150	C
Operating temperature	0 to + 50	C
Supply voltage : V_{DD} - Vss	2	Volt
V_C - Vss	4	Volt
Input voltage range	$V_{SS} < V_{IN} < V_{DD}$	
Output voltage range	$V_{SS} < V_{OUT} < V_{DD}$	
LCD output range	$0 < V_{OUT} < V_C$	

3. Electrical parameters

V_{DD} = 1.5 Volt
Vss = 0.0 Volt
T_A = 25 C
(Voltage doubler connected unless otherwise specified.)

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage (V_{DD})		1.35		1.7	Volt
Supply current (I_{DD})	LCD disconnected			3.0	uA
Doubler output voltage	I_H = 1.0 uA		2.8		Volt
Segment ON voltage	Vc =2.8 V (rms)		2.27		Volt
Segment OFF voltage	Vc =2.8 V (rms)		1.06		Volt
Power consumption				0.02	mW

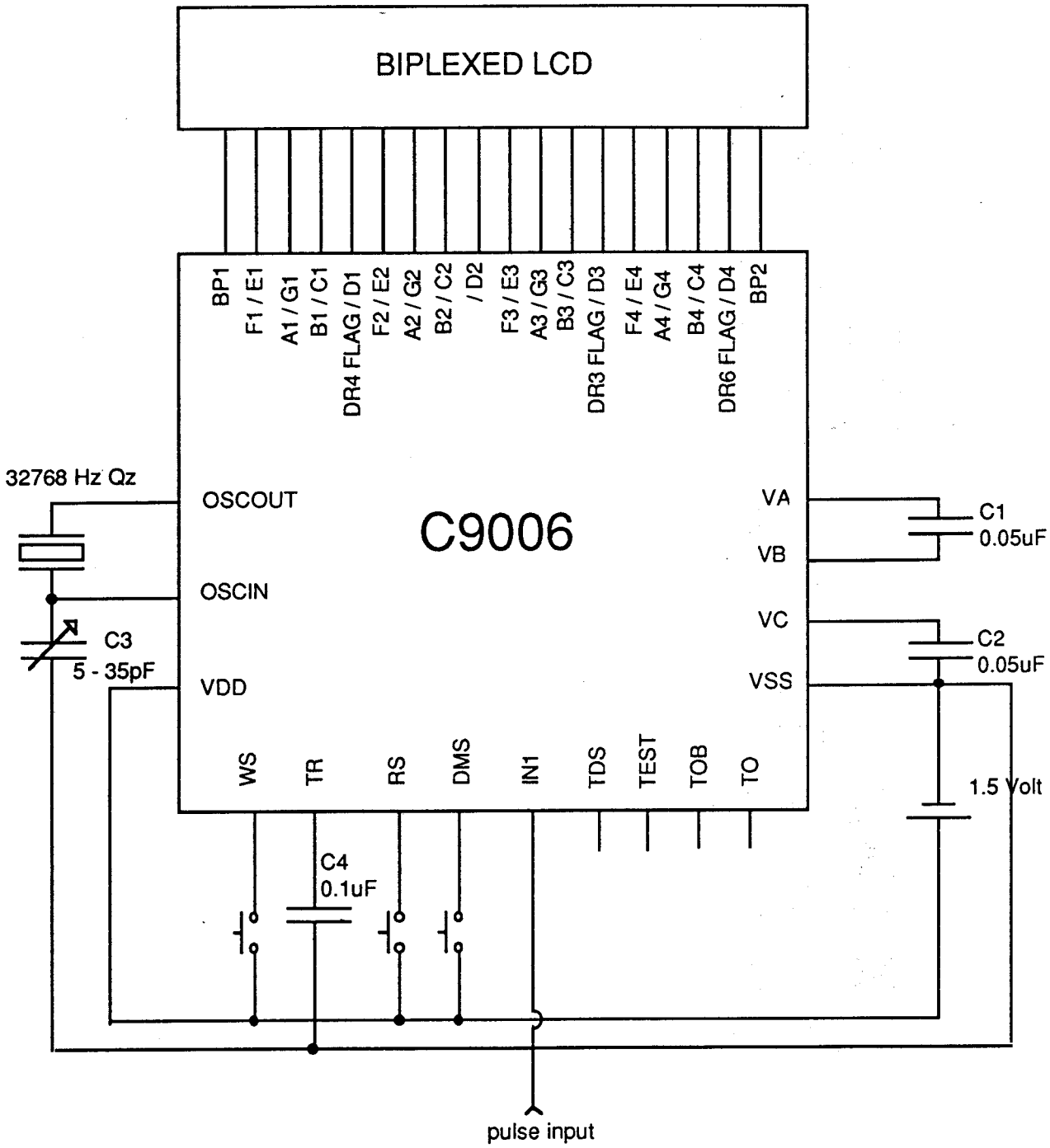
C9006 / PAD DIAGRAM



Low Left Corner's Coordinate For Each Pad

RS	(-1294, -799.05)	F3/E3	(1204, - 48.9)
DMS	(-1294, -992.55)	/D2	(1204, 129.8)
IN1	(- 854.45, -992.55)	B2/C2	(1204, 308.4))
TDS	(- 661.3, -992.55)	A2/G2	(1204, 487.1)
TEST	(- 467.8, -992.55)	F2/E2	(1204, 715.3)
VSS	(- 289.2, -992.55)	DR4FLAG/D1	(1043.4, 902.55)
VC	(- 81.5, -992.55)	B1/C1	(822.95, 902.55)
VB	(98.55, -992.55)	A1/G1	(644.35, 902.55)
VA	(268.55, -992.55)	F1/E1	(465.65, 902.55)
BP2	(448.6, -992.55)	BP1	(269.35, 902.55)
DR6FLAG/D4	(644.35, -992.55)	TOB	(85.45, 902.55)
B4/C4	(822.95, -992.55)	OSCOUT	(-85.65, 902.55)
A4/G4	(1043.4, -992.55)	OSCIN	(-655.2, 902.55)
F4/E4	(1204, -805.3)	VDD	(-860.35, 902.55)
DR3FLAG/D3	(1204, -584.8)	TO	(-1073.75, 902.55)
B3/C3	(1204, -406.2)	WS	(-1294, 763.35)
A3/G3	(1204, -227.5)	TR	(-1294, 570.1)

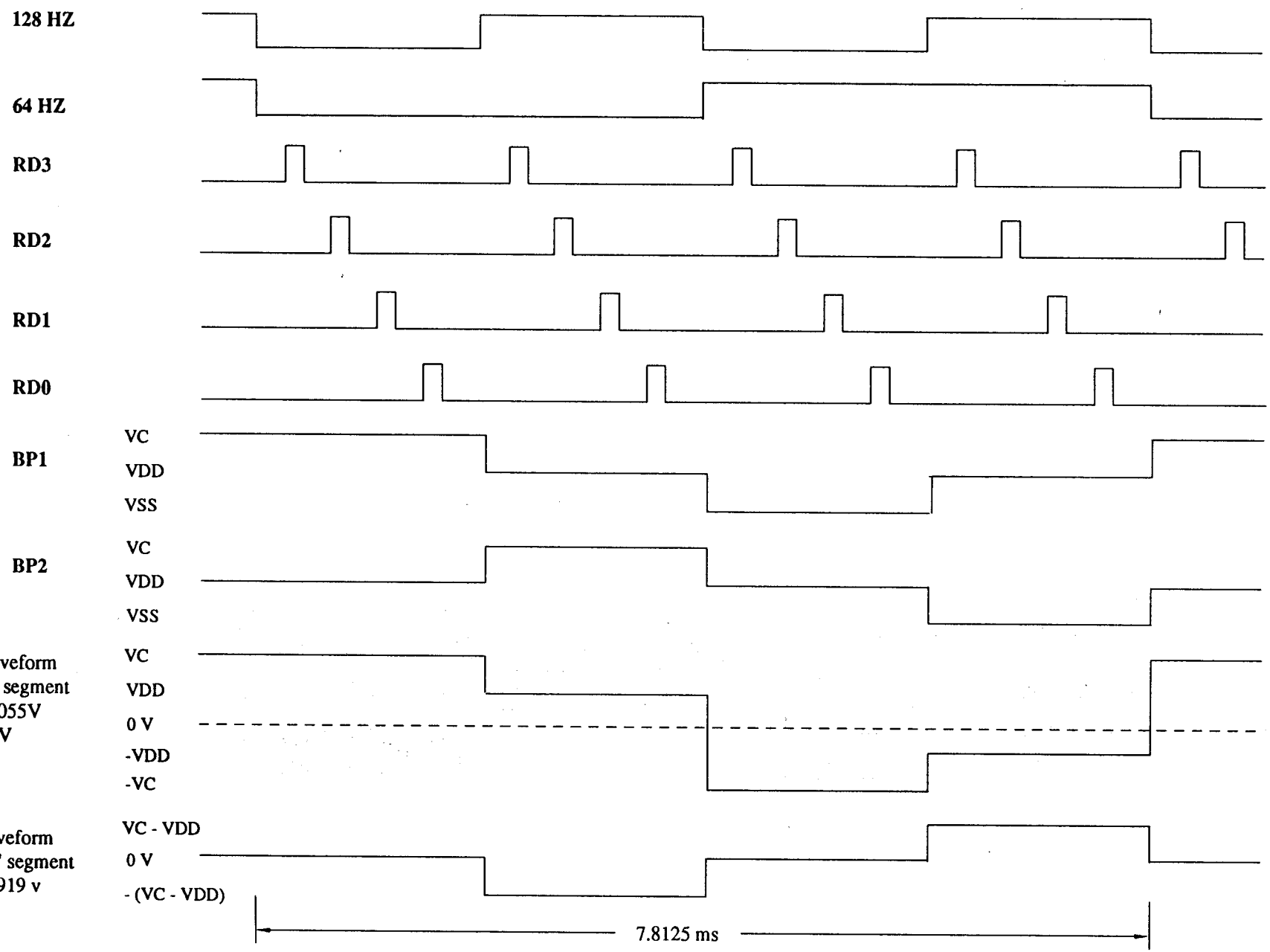
C9006 APPLICATION DIAGRAM



TR - option input with pull-up resistor for testing, connect it to VSS will force the device to power up reset.
TO/TDS/TEST/TOB - option input for wafer testing. They are all connected to Vss during normal application through the internal pull-down resistor. During testing mode, they will be forced to high.

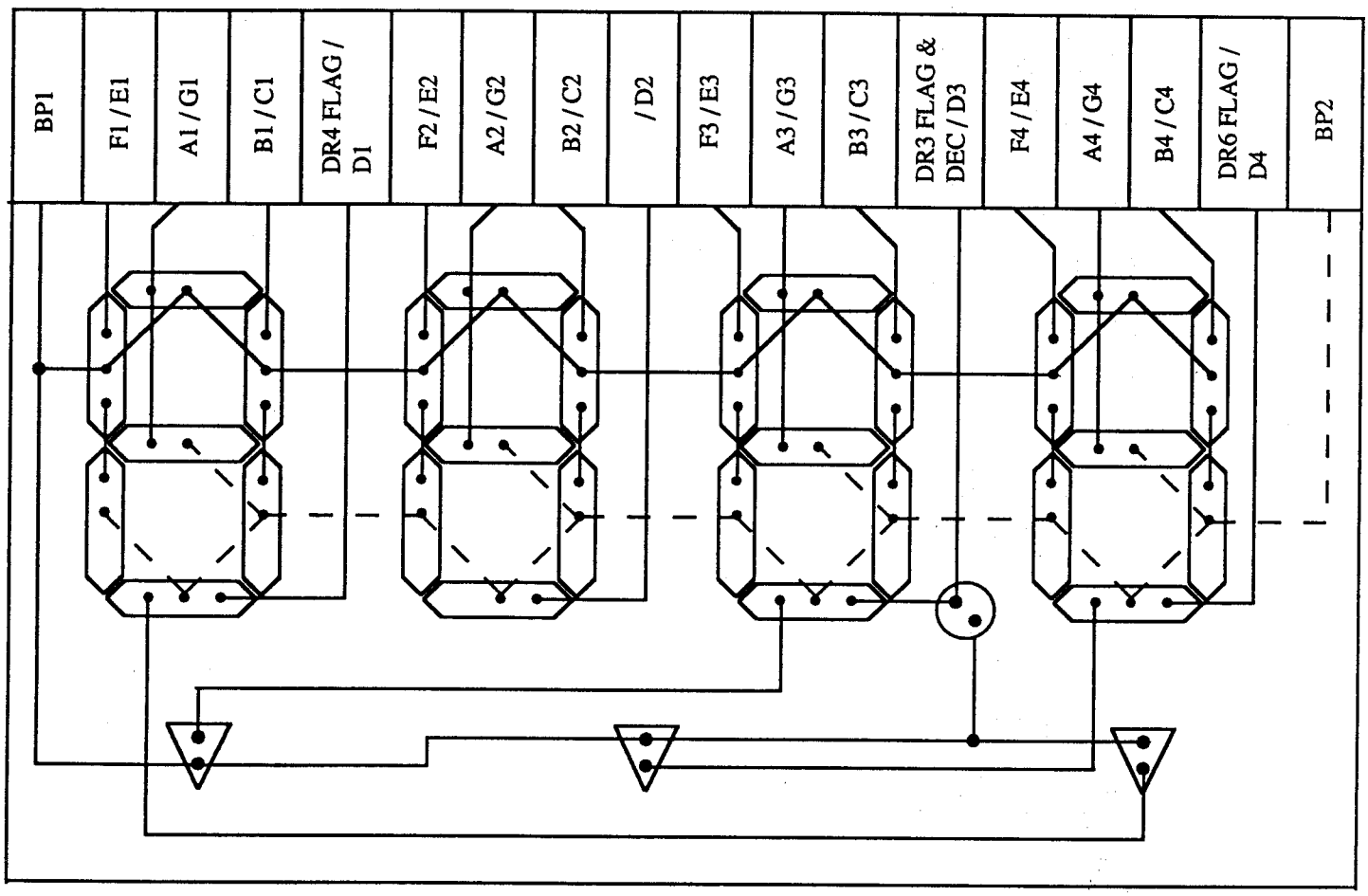
BACKPLANE AND RELATED TIMING

OCT 30, 1994



OCT 30, 1994

LCD FORMAT



16 LCD SEGMENT OUTPUT PADS:

A1 / G1	B1 / C1	F1 / E1	DR4 FLAG / D1
A2 / G2	B2 / C2	F2 / E2	/ D2
A3 / G3	B3 / C3	F3 / E3	DR3 FLAG & DEC / D3
A4 / G4	B4 / C4	F4 / E4	DR6 FLAG / D4

2 LCD BACKPLANES OUTPUT PADS

BP1 BP2

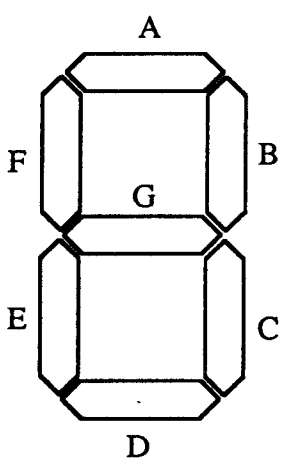
OCT 30, 1994

LCD BIPLEX SEGMENT ARRANGEMENT

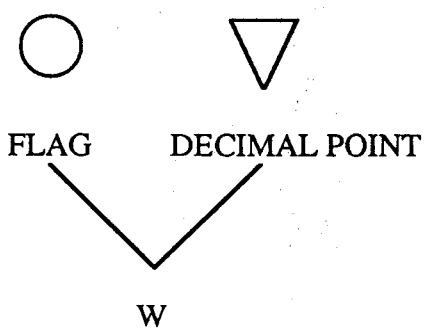
Biplex Segment X1, X2, X3, X4

Common BP1, BP2

	X1	X2	X3	X4
BP1	A	B	W	F
BP2	G	C	D	E



Segment Data



The seven segment data A to G, with one extra bit of information W, combines together to give four biplexed segment outputs