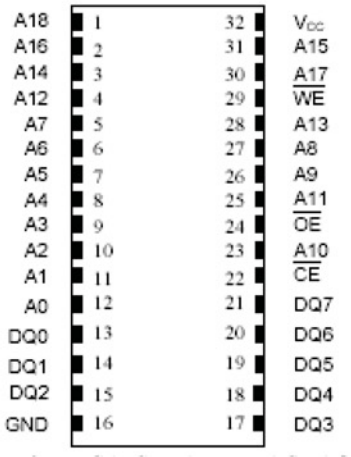
VS1250

4096k Nonvolatile SRAM

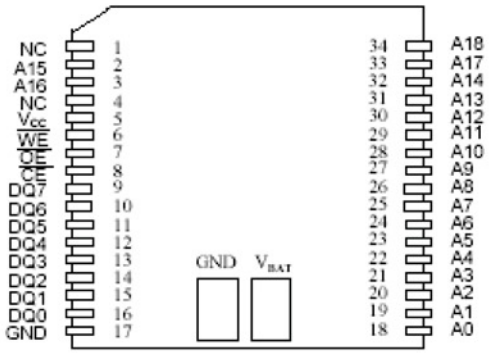
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Replaces 512k x 8 volatile static RAM, EEPROM or Flash memory
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (VS1250Y)
- Optional ±5% V_{CC} operating range (VS1250AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 32-pin DIP package
- PowerCap Module (PCM) package
  - Directly surface-mountable module
  - Replaceable snap-on PowerCap provides lithium backup battery
  - Standardized pinout for all nonvolatile SRAM products
  - Detachment feature on PCM allows easy removal using a regular screwdriver

PIN ASSIGNMENT



32-Pin ENCAPSULATED PACKAGE
740-mil EXTENDED



34-Pin POWERCAP MODULE (PCM)

PIN DESCRIPTION

A0 - A18	- Address Inputs
DQ0 - DQ7	- Data In/Data Out
$\overline{CE}$	- Chip Enable
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
V_{CC}	- Power (+5V)
GND	- Ground

DESCRIPTION

The VS1250 4096k Nonvolatile SRAMs are 4,194,304-bit, fully static, nonvolatile SRAMs organized as 524,288 words by 8 bits. Each complete NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package VS1250 devices can be used in place of existing 512k x 8 static RAMs directly conforming to the popular byte-wide 32-pin DIP standard. VS1250 devices in the PowerCap Module package are directly surface mountable and are normally paired with a PowerCap to form a complete Nonvolatile SRAM module. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The VS1250 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 19 address inputs (A_0–A_{18}) defines which of the 524,288 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later-occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The VS1250 executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$

will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The VS1250AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The VS1250Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high-impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the VS1250AB and 4.5 volts for the VS1250Y.

FRESHNESS SEAL

Each VS1250 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

PACKAGES

The VS1250 is available in two packages: 32-pin DIP and 34-pin PowerCap Module (PCM). The 32-pin DIP integrates a lithium battery, an SRAM memory and a nonvolatile control function into a single package with a JEDEC-standard 600-mil DIP pinout. The 34-pin PowerCap Module integrates SRAM memory and nonvolatile control into a module base along with contacts for connection to the lithium battery PowerCap. The PowerCap Module package design allows a VS1250 PCM device to be surface mounted without subjecting its lithium backup battery to destructive high-temperature reflow soldering. After a VS1250 PCM module base is reflow soldered, a PowerCap is snapped on top of the PCM to form a complete Nonvolatile SRAM module.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature 0°C to 70°C,	-40°C to +85°C for IND parts
Storage Temperature -40°C to +70°C,	-40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

RECOMMENDED DC OPERATING CONDITIONS (t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
VS1250AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
VS1250Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS (t_A: See Note 10)

(V_{CC} =5V ± 5% for VS1250AB)

(V_{CC} =5V ± 10% for VS1250Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ =2.2V	I_{CCS1}		200	600	µA	
Standby Current $\overline{CE}$ =V_{CC}-0.5V	I_{CCS2}		50	150	µA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (VS1250AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (VS1250Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE (t_A =25 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

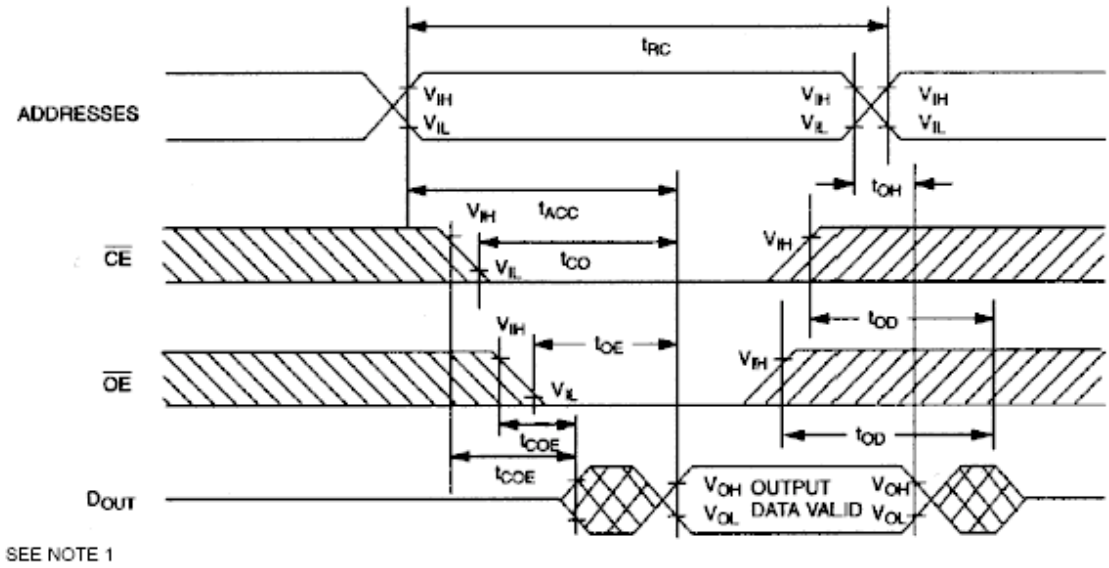
AC ELECTRICAL CHARACTERISTICS

(V_{CC} =5V ± 5% for VS1250AB)

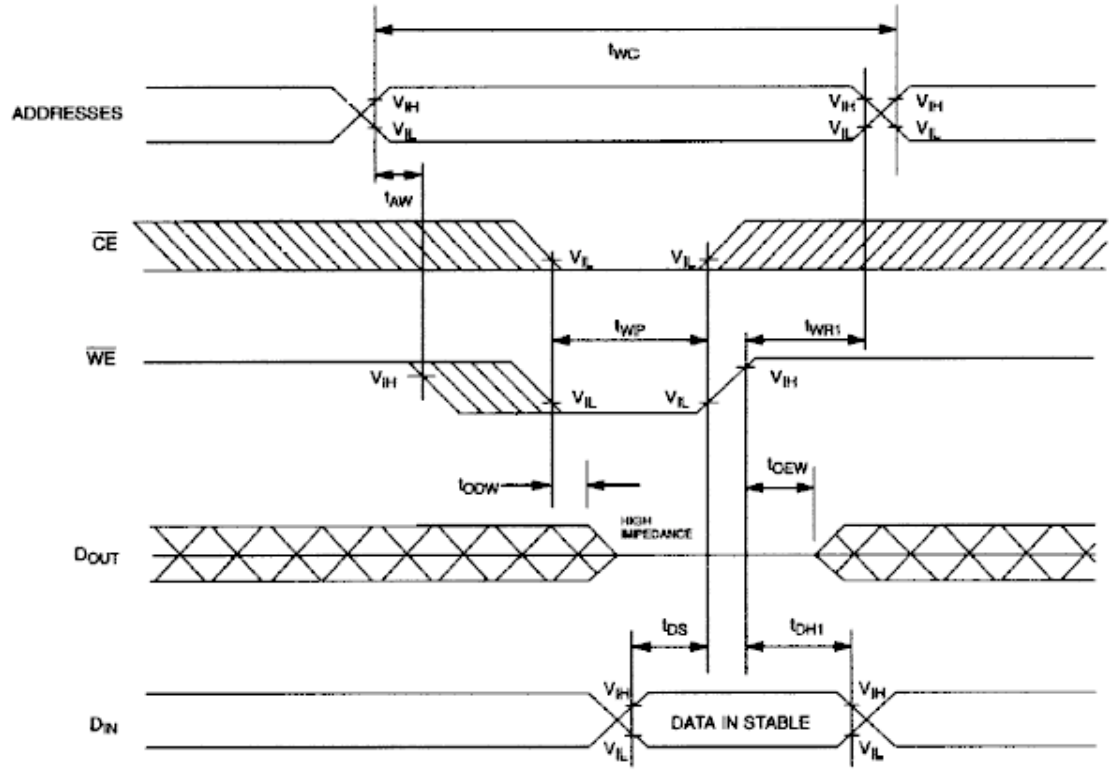
(t_A: See Note 10) (V_{CC} =5V ± 10% for VS1250Y)

PARAMETER	SYMBOL	VS1250—120		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	120		ns	
Access Time	t_{ACC}		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High-Z from Deselection	t_{OD}		40	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	120		ns	
Write Pulse Width	t_{WP}	90		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	20		ns	10
Output High-Z from $\overline{WE}$	t_{ODW}		40	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	50		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		ns	4

READ CYCLE

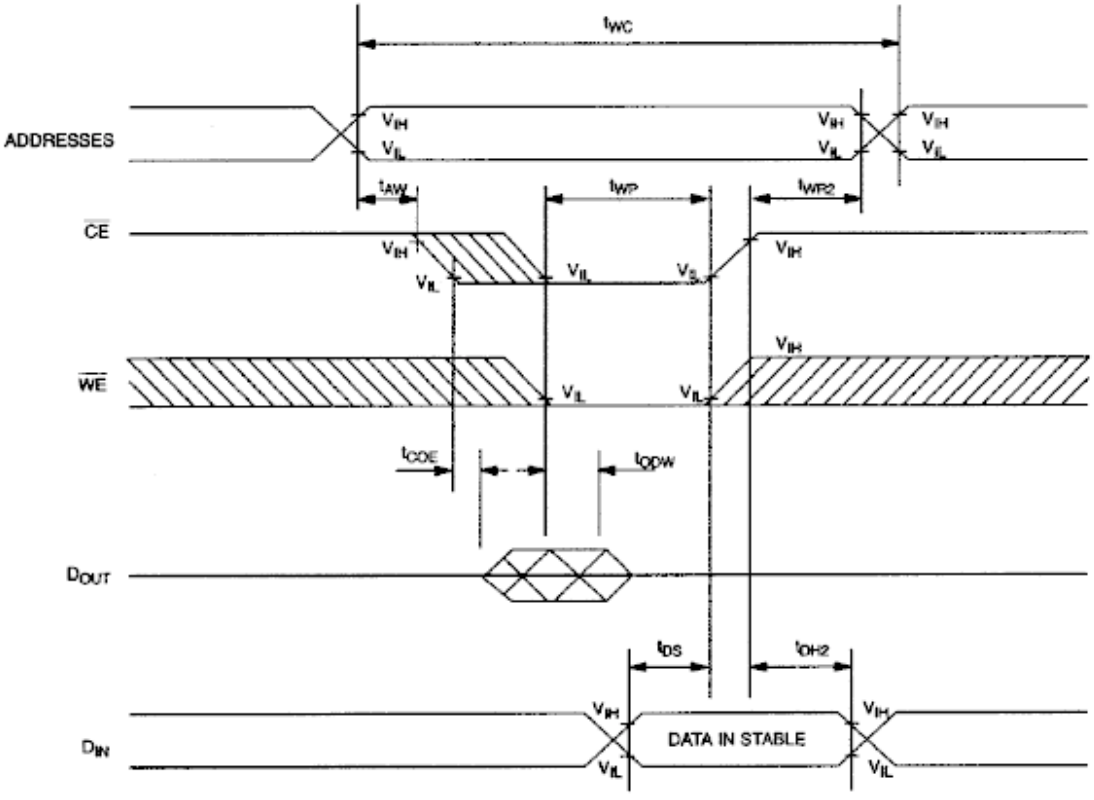


WRITE CYCLE 1



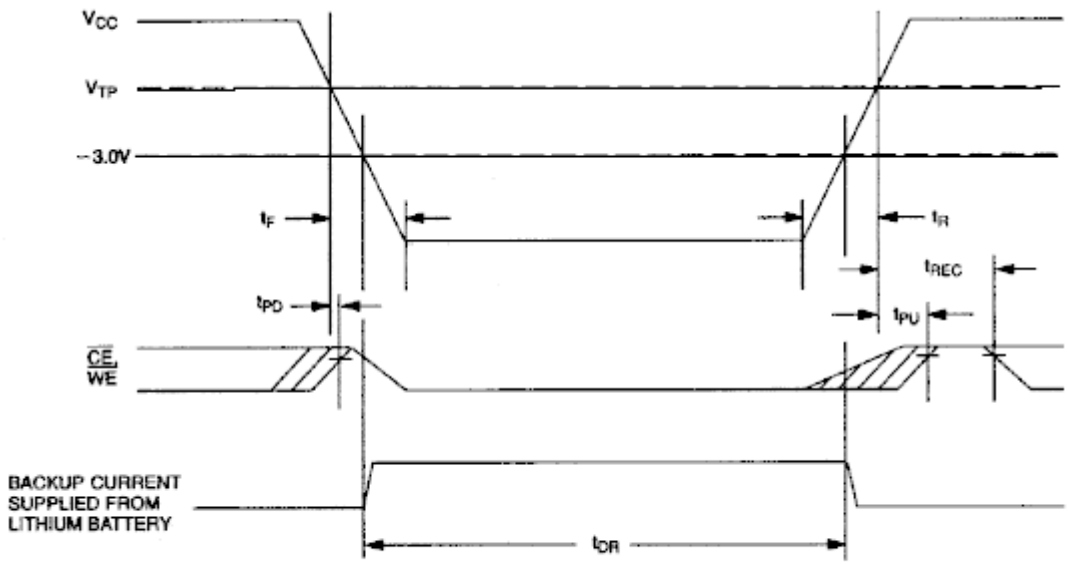
SEE NOTES 2, 3, 4, 6, 7, 8, and 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8, and 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING (t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	11
V_{CC} slew from V_{TP} to 0V	t_F	150			µs	
V_{CC} slew from 0V to V_{TP}	t_R	150			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(t_A =25 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.

2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a

high-impedance state.

3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high-impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
9. Each VS1250 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power-down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.

DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

VS1250 TTP - SSS - III

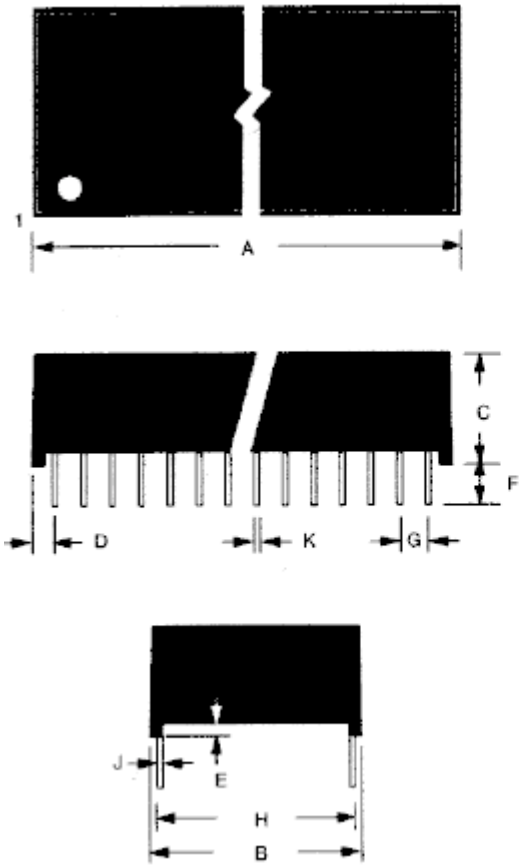
Operating Temperature Range
- blank: 0° to 70°
- IND: -40° to +85°C

Access Speed
- 70: 70 ns
- 100: 100 ns

Package Type
- blank: 32-pin 600 mil DIP
- P: 34-pin PowerCap Module

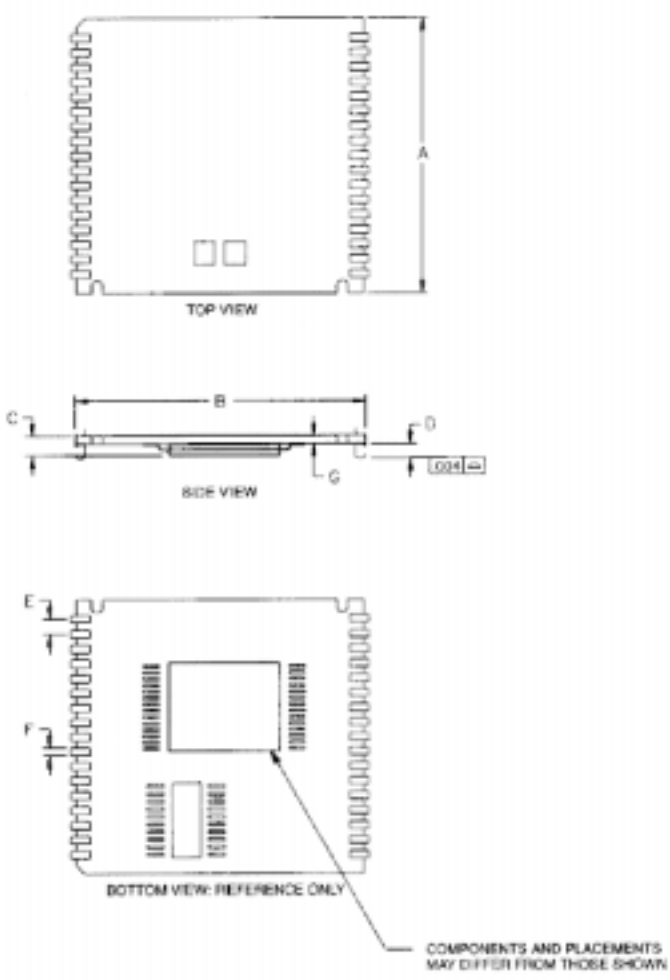
Device Type
- AB: ±5%
- Y: ±10%

VS1250Y/AB NONVOLATILE SRAM, 32-PIN, 740 MIL-EXTENDED DIP MODULE



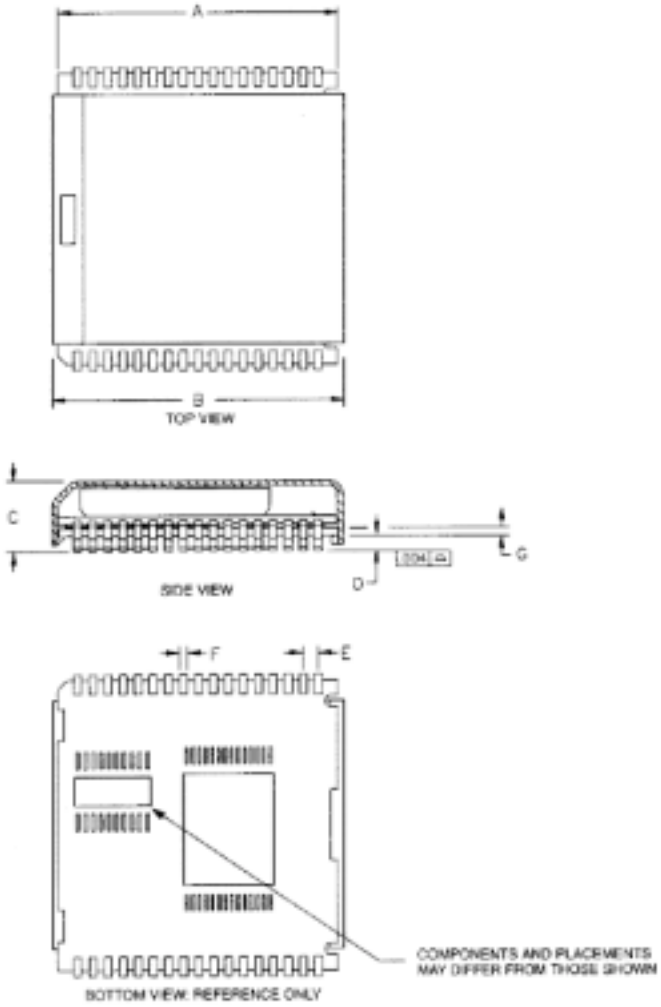
PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

VS1250Y/AB NONVOLATILE SRAM, 34-PIN POWERCAP MODULE



PKG DIM	INCHES		
	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.980	0.985	0.990
C	-	-	0.080
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030

VS1250Y/AB NONVOLATILE SRAM, 34-PIN POWERCAP MODULE WITH POWERCAP



PKG DIM	INCHES		
	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.955	0.960	0.965
C	0.240	0.245	0.250
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030

ASSEMBLY AND USE

Reflow soldering

recommends that PowerCap Module bases experience one pass through solder reflow oriented label-side up (live-bug).

Hand soldering and touch-up

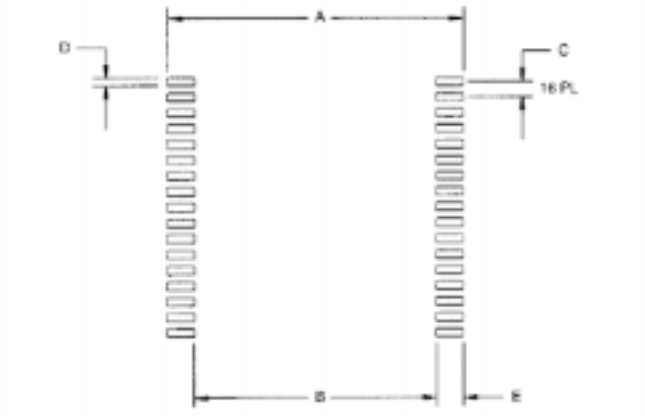
Do not touch soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove part, apply flux, heat pad until solder reflows, and use a solder wick.

LPM replacement in a socket

To replace a Low Profile Module in a 68-pin PLCC socket, attach a PowerCap to a module base then insert the complete module into the socket one row of leads at a time, pushing only

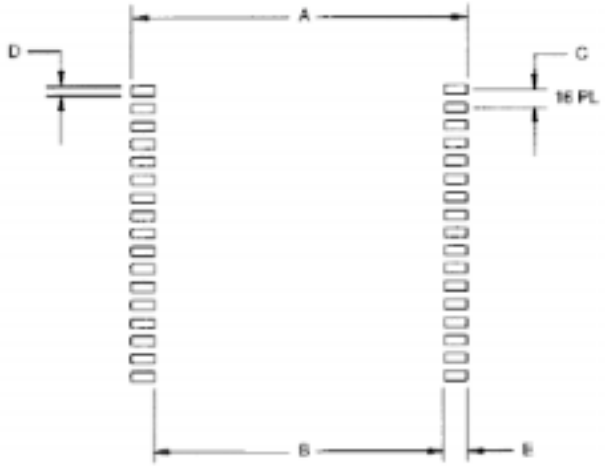
on the corners of the cap. Never apply force to the center of the device. To remove from a socket, use a PLCC extraction tool and ensure that it does not hit or damage any of the module IC components. Do not use any other tool for extraction.

RECOMMENDED POWERCAP MODULE LAND PATTERN



PKG DIM	INCHES		
	MIN	NOM	MAX
A	-	1.050	-
B	-	0.826	-
C	-	0.050	-
D	-	0.030	-
E	-	0.112	-

RECOMMENDED POWERCAP MODULE SOLDER STENCIL



PKG DIM	INCHES		
	MIN	NOM	MAX
A	-	1.050	-
B	-	0.890	-
C	-	0.050	-
D	-	0.030	-
E	-	0.080	-