



## Nonvolatile Timekeeping RAM

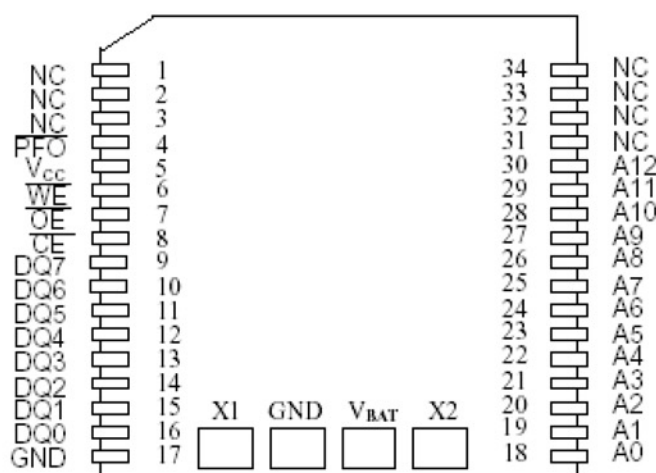
### FEATURES

- Integrated NV SRAM, real time clock, crystal, power-fail control circuit and lithium energy source
- Clock registers are accessed identically to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 70 ns and 100 ns
- BCD coded year, month, date, day, hours, minutes, and seconds with leap year compensation valid up to 2100
- Power-fail write protection allows for  $\pm 10\%$   $V_{CC}$  power supply tolerance
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- VS1643 only (DIP Module)
  - Standard JEDEC byte-wide 8K x 8 RAM pinout
- VS1643P only (PowerCap Module Board)
  - Surface mountable package for direct connection to PowerCap containing battery and crystal
  - Replaceable battery (PowerCap)
  - Power-fail output

### PIN ASSIGNMENT

NC	1	28	VCC
A12	2	27	$\overline{WE}$
A7	3	26	CE2
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
GND	14	15	DQ3

28-PIN Encapsulated Package  
(700-mil Extended)



34-PIN PowerCap Module Board

## ORDERING INFORMATION

VS1643-XXX      28-pin DIP module  
                     -70      70 ns access  
                     -100     100 ns access

\*VS1643P-XXX    34-pin PowerCap Module Board  
                     -70      70 ns access  
                     -100     100 ns access

## PIN DESCRIPTION

A0-A12	- Address Input	GND	- Ground
$\overline{CE}$	- Chip Enable	DQ0-DQ7	- Data Input/Output
CE2	- Chip Enable 2 (DIP Module only)	NC	- No Connect
$\overline{OE}$	- Output Enable	$\overline{RST}$	- Power-on Reset Output (PowerCap Module board only)
$\overline{WE}$	- Write Enable	X1, X2	- Crystal Connection
V <sub>CC</sub>	- +5 Volts	V <sub>BAT</sub>	- Battery Connection

## DESCRIPTION

The VS1643 is a 8K x 8 nonvolatile static RAM with a full function Real Time Clock (RTC) which are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The VS1643 also contains its own power-fail circuitry which deselects the device when the V<sub>CC</sub> supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V<sub>CC</sub> as errant access and update cycles are avoided.

## PACKAGES

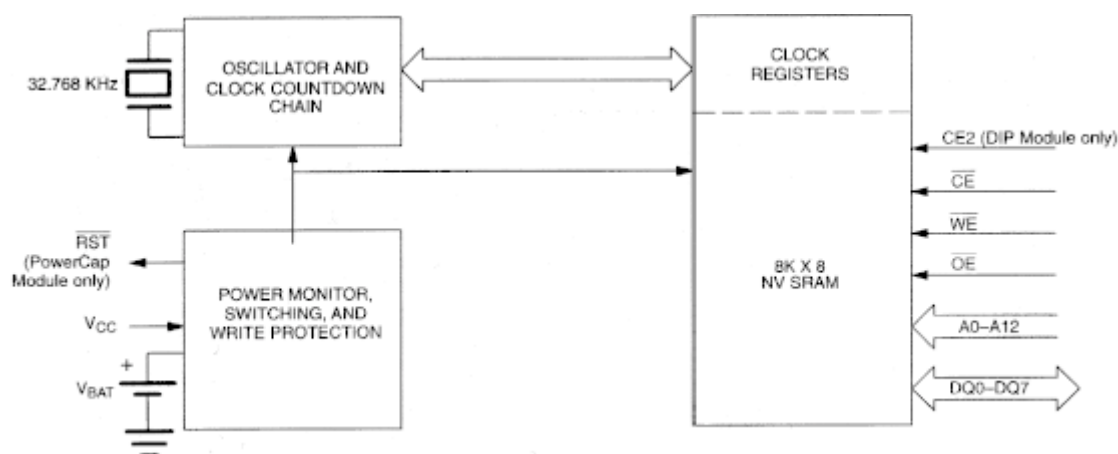
The VS1643 is available in two packages: 28-pin DIP module and 34-pin PowerCap module. The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the VS1643P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and

PowerCap are ordered separately and shipped in separate containers.

## CLOCK OPERATIONS-READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the VS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a one is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the VS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

## BLOCK DIAGRAM VS1643 Figure 1



## VS1643 TRUTH TABLE Table 1

V <sub>CC</sub>	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V <sub>IH</sub>	X	X	X	DESELECT	HIGH Z	STANDBY
	X	V <sub>IL</sub>	X	X	DESELECT	HIGH Z	STANDBY
	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>IL</sub>	WRITE	DATA IN	ACTIVE
	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	READ	DATA OUT	ACTIVE
	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V <sub>BAT</sub>	X	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V <sub>BAT</sub>	X	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

## SETTING THE CLOCK

The 8-bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the VS1643 registers. The user can then load them with the correct day, date and time data in 24 hour

BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The  $\overline{OSC}$  bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

## FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e.,  $\overline{CE}$  low,  $\overline{OE}$  low, CE2 high, and address for seconds register remain valid and stable).

## CLOCK ACCURACY (DIP MODULE)

The VS1643 is guaranteed to keep time accuracy to within  $\pm 1$  minute per month at 25°C.

## CLOCK ACCURACY (POWERCAP MODULE)

The VS1643P and POWERCAP are each individually tested for accuracy. Once mounted together, the module is guaranteed to keep time accuracy to within  $\pm 1.53$  minutes per month (35 ppm) at 25°C.

## VS1643 REGISTER MAP - BANK1 Table 2

ADDRESS S	DATA								FUNCTION
	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	
1FFF	-	-	-	-	-	-	-	-	YEAR 00-99
1FFE	X	X	X	-	-	-	-	-	MONTH 01-12
1FFD	X	X	-	-	-	-	-	-	DATE 01-31
1FFC	X	FT	X	X	X	-	-	-	DAY 01-07
1FFB	X	X	-	-	-	-	-	-	HOUR 00-23
1FFA	X	-	-	-	-	-	-	-	MINUTES 00-59
1FF9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS 00-59
1FF8	W	R	X	X	X	X	X	X	CONTROL A

$\overline{OSC}$  = STOP BIT  
W = WRITE BIT

R = READ BIT  
X = UNUSED

FT = FREQUENCY TEST

## NOTE:

All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

## RETRIEVING DATA FROM RAM OR CLOCK

The VS1643 is in the read mode whenever  $\overline{WE}$  (write enable) is high and  $\overline{CE}$  (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within  $t_{AA}$  after the last address input is stable, providing that the  $\overline{CE}$  and  $\overline{OE}$  access times and states are satisfied. If  $\overline{CE}$  or  $\overline{OE}$  access times are not met, valid data will be available at the latter of chip enable access ( $t_{CEA}$ ) or at output enable access time ( $t_{OEA}$ ). The state of the data input/output pins (DQ) is controlled by  $\overline{CE}$  and  $\overline{OE}$ . If the outputs are activated before  $t_{AA}$ , the data lines are driven to an intermediate state until  $t_{AA}$ . If the address inputs are changed while  $\overline{CE}$  and  $\overline{OE}$  remain valid, output data will remain valid for output data hold time ( $t_{OH}$ ) but will then go indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The VS1643 is in the write mode whenever  $\overline{WE}$  and  $\overline{CE}$  are in their active state. The start of a write is referenced to the latter occurring transition of  $\overline{WE}$  or  $\overline{CE}$ . The addresses must be held valid throughout the cycle.  $\overline{CE}$  or  $\overline{WE}$  must return inactive for a minimum of  $t_{WR}$  prior to the initiation of another read or write cycle. Data in must be valid  $t_{DS}$  prior to the end of write and remain valid for  $t_{DH}$  afterward. In a typical application, the  $\overline{OE}$  signal will be high during a write cycle. However,  $\overline{OE}$  can be active provided that care is taken with the data bus to avoid bus contention. If  $\overline{OE}$  is low prior to  $\overline{WE}$  transitioning low the data bus can become active with read data defined by the address inputs. A low transition on  $\overline{WE}$  will then disable the outputs  $t_{WEZ}$  after  $\overline{WE}$  goes active.

## DATA RETENTION MODE

When  $V_{CC}$  is within nominal limits ( $V_{CC} > 4.5$  volts) the VS1643 can be accessed as described above with read or write cycles. However, when  $v_{cc}$  is below the power-fail point  $V_{PF}$  (point at which write protection occurs) the internal clock registers and RAM are blocked from access. This is accomplished internally by inhibiting access via the  $\overline{CE}$  signal. At this time the power-on reset output signal ( $\overline{RST}$ ) will be driven active low and will remain active until  $V_{CC}$  returns to nominal levels. When  $v_{cc}$  falls below the level of the internal battery supply, power input is switched from the  $V_{CC}$  pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until  $V_{CC}$  is returned to nominal level. The  $\overline{RST}$  signal is an open drain output and requires a pull up. Except for the  $\overline{RST}$ ,

all control, data, and address signals must be powered down when  $V_{CC}$  is powered down.

## BATTERY LONGEVITY

The VS1643 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the  $V_{CC}$  supply is not present. The capability of this internal power supply is sufficient to power the VS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of  $V_{CC}$  power. Each VS1643 is shipped with its lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is first applied at a level greater than  $V_{PF}$ , the lithium energy source is enabled for battery backup operation. Actual life expectancy of the VS1643 will be much longer than 10 years since no lithium battery energy is consumed when  $V_{CC}$  is present.

## ABSOLUTE MAXIMUM RATINGS\*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Soldering Temperature	J-STD-020A Specification (See Note 7)

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS (0°C to 7°C)

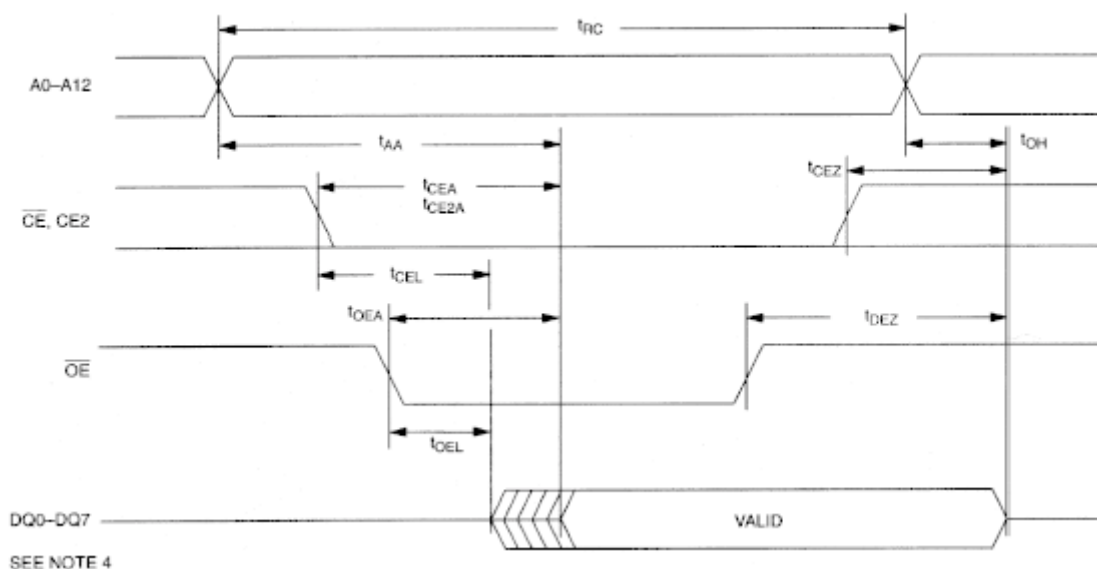
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs	$V_{IH}$	2.2		$V_{CC}+0.3$	V	
Logic 0 Voltage All Inputs	$V_{IL}$	-0.3		0.8	V	

## DC ELECTRICAL CHARACTERISTICS (0°C to 7°C; $V_{CC} = 5.0V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	$I_{CC}$		15	50	mA	2, 3
TTL Standby Current ( $\overline{CE} = V_{IH}$ , $CE2 = V_{IL}$ )	$I_{CC1}$		1	3	mA	2, 3
CMOS Standby Current ( $\overline{CE} = V_{CC} - 0.2V$ , $CE2 = GND + 0.2V$ )	$I_{CC2}$		1	3	mA	2, 3
Input Leakage Current (any input)	$I_{IL}$	-1		+1	$\mu A$	
Output Leakage Current (any output)	$I_{OL}$	-1		+1	$\mu A$	
Output Logic 1 Voltage ( $I_{OUT} = -1.0$ mA)	$V_{OH}$	2.4				1
Output Logic 0 Voltage ( $I_{OUT} = +2.1$ mA)	$V_{OL}$			0.4		1
Write Protection Voltage	$V_{PF}$	4.25	4.37	4.50	V	1

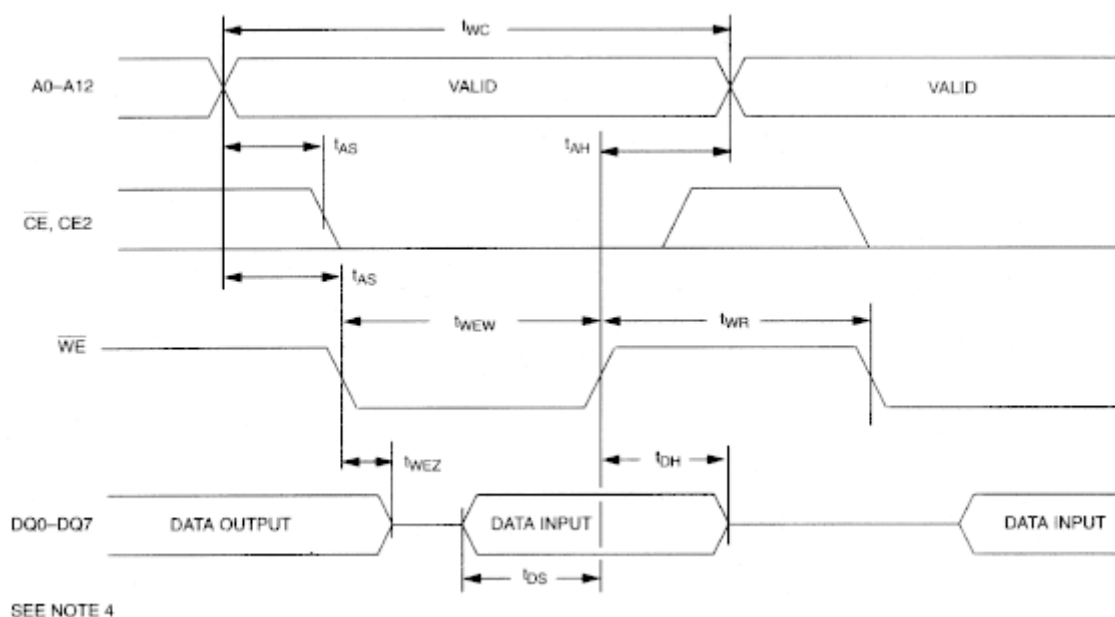
**READ CYCLE, AC CHARACTERISTICS**(0°C to 7°C;  $V_{CC} = 5.0V \pm 10\%$ )

PARAMETER	SYMBOL	70 ns access		100 ns access		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	$t_{RC}$	70		100		ns	4
Address Access Time	$t_{AA}$		70		100	ns	4
$\overline{CE}$ and CE2 to DQ Low-Z	$t_{CEL}$	5		5		ns	4
$\overline{CE}$ Access Time	$t_{CEA}$		70		100	ns	4
CE2 Access Time	$t_{CE2A}$		80		105	ns	4
$\overline{CE}$ and CE2 Data Off Time	$t_{CEZ}$		25		35	ns	4
$\overline{OE}$ to DQ Low-Z	$t_{OEL}$	5		5		ns	4
$\overline{OE}$ Access Time	$t_{OEA}$		35		55	ns	4
$\overline{OE}$ Data Off Time	$t_{OEZ}$		25		35	ns	4
Output Hold from Address	$t_{OH}$	5		5		ns	4

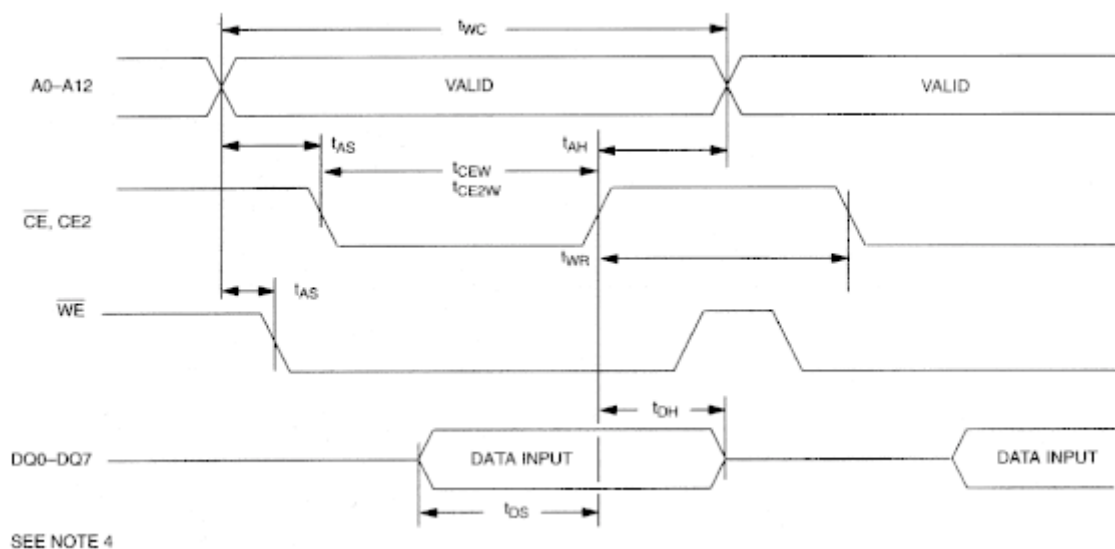
**READ CYCLE TIMING DIAGRAM****WRITE CYCLE, AC CHARACTERISTICS**(0°C to 7°C;  $V_{CC} = 5.0V \pm 10\%$ )

PARAMETER	SYMBOL	70 ns access		100 ns access		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	$t_{WC}$	70		100		ns	4
Address Setup Time	$t_{AS}$	0		0		ns	4
$\overline{WE}$ Pulse Width	$t_{WEW}$	50		70		ns	4
$\overline{CE}$ Pulse Width	$t_{CEW}$	60		75		ns	4
CE2 Pulse Width	$t_{CE2W}$	65		85		ns	4
Data Setup Time	$t_{DS}$	30		40		ns	4
Data Hold Time	$t_{DH}$	0		0		ns	4
Address Hold Time	$t_{AH}$	5		5		ns	4
$\overline{WE}$ Data Off Time	$t_{WEZ}$		25		35	ns	4
Write Recovery Time	$t_{WR}$	5		5		ns	4

## WRITE CYCLE TIMING DIAGRAM, WRITE-ENABLE CONTROLLED



## WRITE CYCLE TIMING DIAGRAM, $\overline{CE}$ , CE2 CONTROLLED

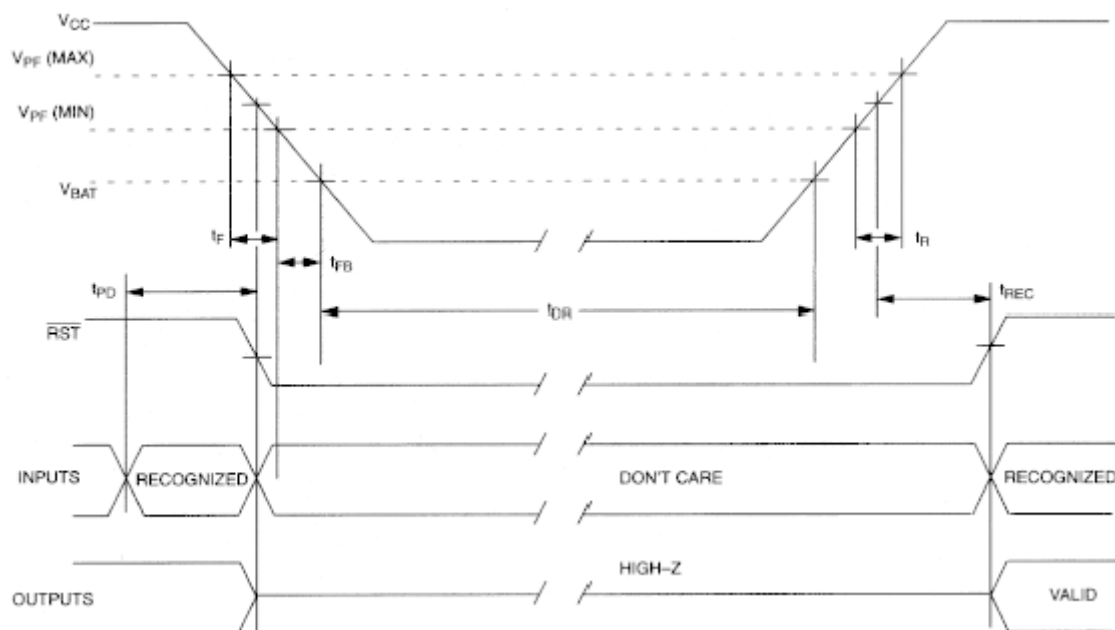


## POWER-UP/DOWN AC CHARACTERISTICS (0°C to 7°C; $V_{CC} = 5.0V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ , CE2 at $V_{IL}$ , Before Power-down	$t_{PD}$	0			$\mu s$	
$V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	$t_F$	300			$\mu s$	
$V_{CC}$ Fall Time: $V_{PF(MIN)}$ to $V_{BAT}$	$t_{FB}$	10			$\mu s$	
$V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	$t_R$	0			$\mu s$	
Power-up Recover Time	$t_{REC}$			35	ms	
Expected Data Retention Time (Oscillator On)	$t_{DR}$	10			years	5, 6



## POWER-UP/POWER-DOWN TIMING



## CAPACITANCE

( $T_A = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins	$C_{IN}$			7	pF	
Capacitance on all output pins	$C_O$			10	pF	

## AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate

Input Pulse Levels: 0.0 to 3.0 Volts

Timing Measurement Reference Levels:

Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5 ns

## NOTES:

1. Voltages are referenced to ground.
2. Typical values are at  $25^\circ\text{C}$  and nominal supplies.
3. Outputs are open.
4. The CE2 control signal functions exactly the same as the  $\overline{CE}$  signal except that the logic levels for active and inactive levels are opposite.
5. Data retention time is at  $25^\circ\text{C}$ .
6. Each VS1643 has a built-in switch that disconnects the lithium source until  $V_{CC}$  is first applied by the user. The expected  $t_{DR}$  is defined for DIP modules as a cumulative time in the absence of  $V_{CC}$  starting

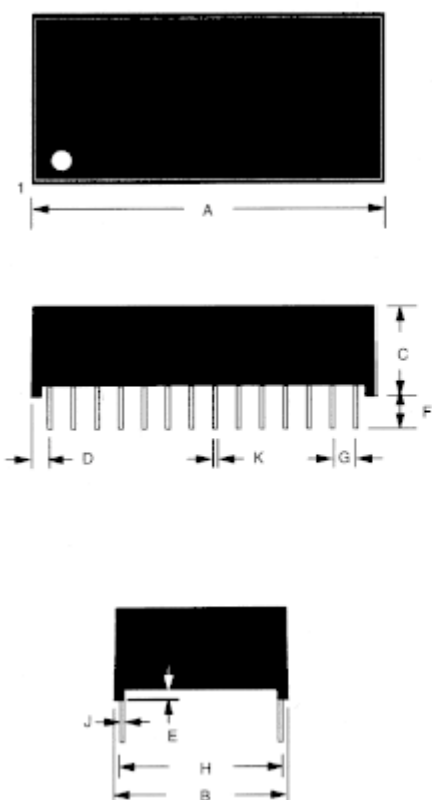
from the time power is first applied by the user.

7. Real-Time Clock Modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

In addition, for the PowerCap:

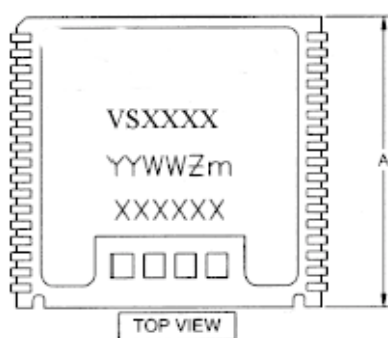
- recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
- Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflow and use a solder wick to remove solder.

## VS1643P

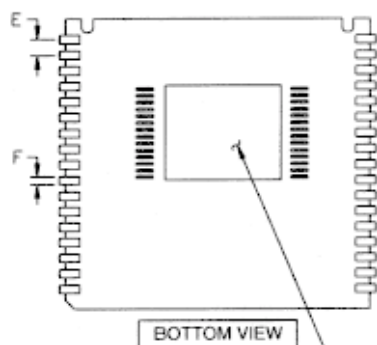
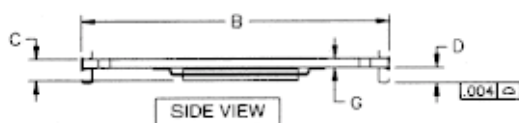


PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.470	1.490
MM	37.34	37.85
B IN.	0.675	0.740
MM	17.75	18.80
C IN.	0.315	0.335
MM	8.51	9.02
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

## VS1643P



PKG DIM	INCHES		
	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.980	0.985	0.990
C	-	-	0.080
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.025	0.027	0.030



COMPONENTS AND PLACEMENT MAY  
VARY FROM EACH DEVICE TYPE

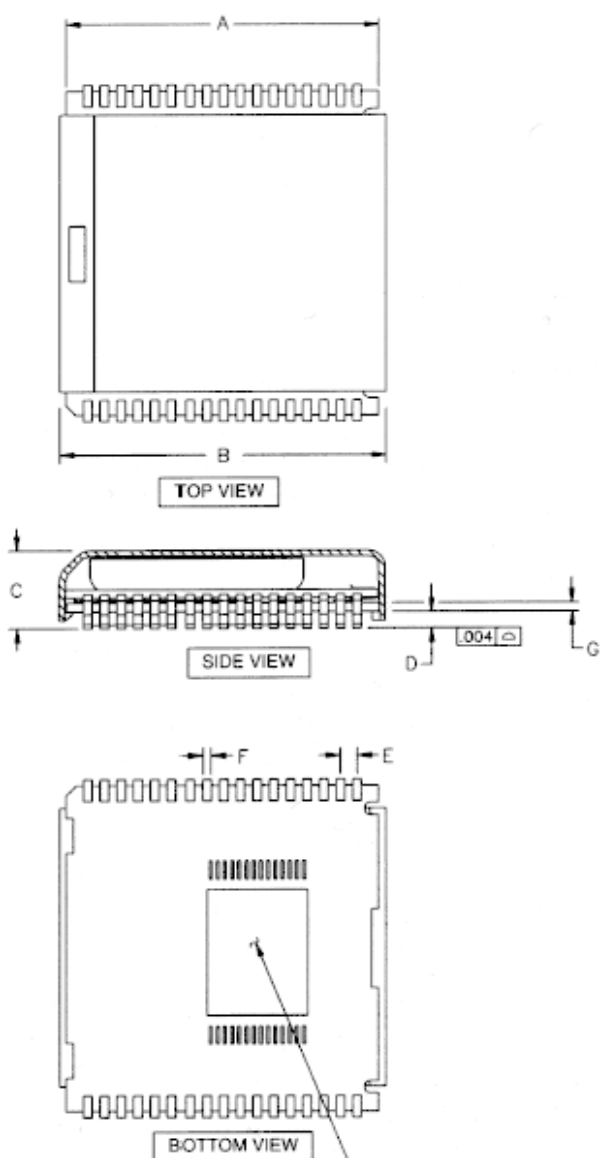
**NOTE:**

recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).

Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 (three) seconds.

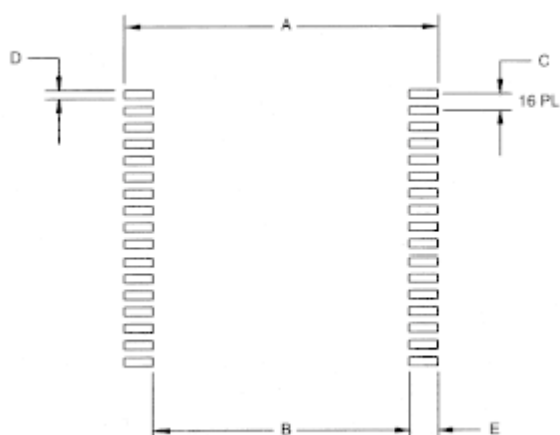
To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.

### VS1643P WITH POWERCAP ATTACHED



PKG DIM	INCHES		
	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.955	0.960	0.965
C	0.240	0.245	0.250
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030

### RECOMMENDED POWERCAP MODULE LAND PATTERN



PKG DIM	INCHES		
	MIN	NOM	MAX
A	-	1.050	-
B	-	0.826	-
C	-	0.050	-
D	-	0.030	-
E	-	0.112	-