**VOSSEL**

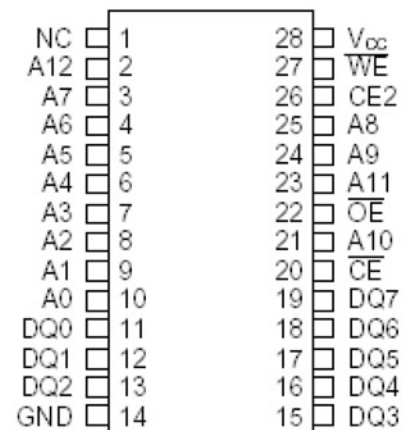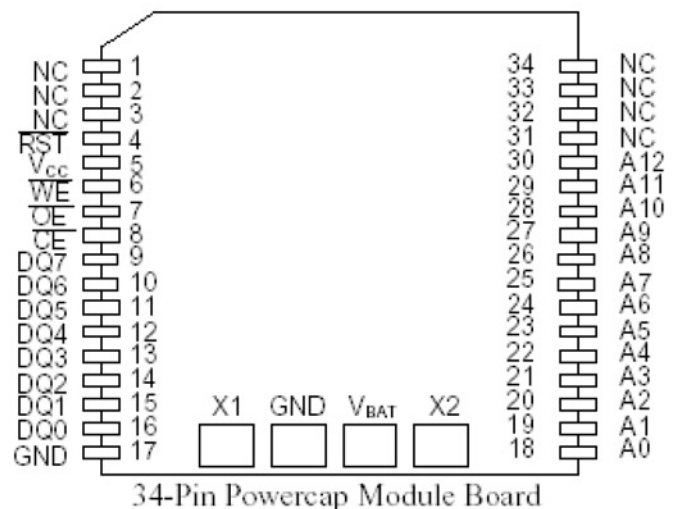# VS1743
## Y2KC Nonvolatile Timekeeping RAM

# FEATURES

- Integrated NV SRAM, real time clock, crystal, power-fail control circuit and lithium energy source
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Century byte register
- Totally nonvolatile with over 10 years of operation in
- the absence of power
- BCD coded century, year, month, date, day, hours, minutes, and seconds with automatic leap year compensation valid up to the year 2100
- Battery voltage level indicator flag
- Power-fail write protection allows for $\pm10\%$ $V_{CC}$ power supply tolerance
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- DIP Module only
  _Standard JEDEC bytewide 8k x 8 static RAM pinout
- PowerCap Module Board only
  _Surface mountable package for direct connection to PowerCap containing battery and crystal
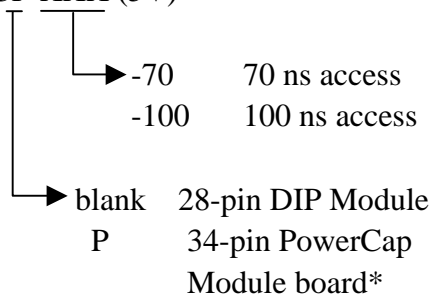  _Replaceable battery (PowerCap)
  _Power-On Reset Output

# PIN ASSIGNMENT



| NC | 1 | 28 | $V_{CC}$ |
|----|---|----|----------|
| A12 | 2 | 27 | $\overline{WE}$ |
| A7 | 3 | 26 | CE2 |
| A6 | 4 | 25 | A8 |
| A5 | 5 | 24 | A9 |
| A4 | 6 | 23 | A11 |
| A3 | 7 | 22 | $\overline{OE}$ |
| A2 | 8 | 21 | A10 |
| A1 | 9 | 20 | $\overline{CE}$ |
| A0 | 10 | 19 | DQ7 |
| DQ0 | 11 | 18 | DQ6 |
| DQ1 | 12 | 17 | DQ5 |
| DQ2 | 13 | 16 | DQ4 |
| GND | 14 | 15 | DQ3 |

28-Pin Encapsulated Package
(700-mil Extended)



| NC | 1 | 34 | NC |
|----|---|----|----|
| NC | 2 | 33 | NC |
| NC | 3 | 32 | NC |
| RST | 4 | 31 | NC |
| $V_{CC}$ | 5 | 30 | A12 |
| $\overline{WE}$ | 6 | 29 | A11 |
| $\overline{OE}$ | 7 | 28 | A10 |
| $\overline{CE}$ | 8 | 27 | A9 |
| DQ7 | 9 | 26 | A8 |
| DQ6 | 10 | 25 | A7 |
| DQ5 | 11 | 24 | A6 |
| DQ4 | 12 | 23 | A5 |
| DQ3 | 13 | 22 | A4 |
| DQ2 | 14 | 21 | A3 |
| DQ1 | 15 | 20 | A2 |
| DQ0 | 16 | 19 | A1 |
| GND | 17 | 18 | A0 |

X1  GND  $V_{BAT}$  X2

34-Pin Powercap Module Board

## ORDERING INFORMATION

VS1743P-XXX (5V)

-70  70 ns access
-100  100 ns access

blank 28-pin DIP Module
P  34-pin PowerCap
   Module board*

VS1743WP-XXX (3.3V)

-120 120 ns access
-150 150 ns access

blank 28-pin DIP Module
P  34-pin PowerCap
   Module board*
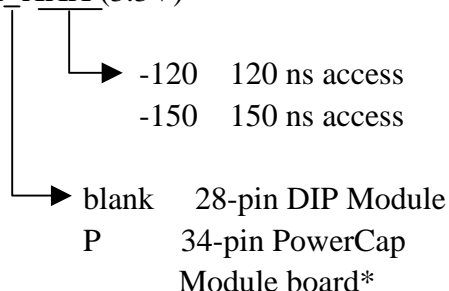
## PIN DESCRIPTION

| | |
|---|---|
| A0-A12 | - Address Input |
| $\overline{CE}$ | - Chip Enable |
| CE2 | - Chip Enable 2 (DIP Module only) |
| $\overline{OE}$ | - Output Enable |
| $\overline{WE}$ | - Write Enable |
| $V_{CC}$ | - Power Supply Input |
| GND | - Ground |
| DQ0-DQ7 | - Data Input/Output |
| NC | - No Connection |
| $\overline{RST}$ | - Power-On Reset Output (PowerCap Module board only) |
| X1, X2 | - Crystal Connection |
| $V_{BAT}$ | - Battery Connection |

## DESCRIPTION

The VS1743 is a full function, year 2000-compliant (Y2KC), real-time clock/calendar (RTC) and 8k x 8 non-volatile static RAM. User access to all registers within the VS1743 is accomplished with a bytewide interface as shown in Figure 1. The Real Time Clock (RTC) information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The VS1743 also contains its own power-fail circuitry, which deselects the device when the $V_{CC}$ supply is in an out of tolerance
condition. This feature prevents loss of data from unpredictable system operation brought on by low $V_{CC}$ as errant access and update cycles are avoided.

## PACKAGES

The VS1743 is available in two packages (28-pin DIP and 34-pin PowerCap module). The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap that contains the crystal and   battery. This design allows the PowerCap to be mounted on top of the VS1743P after the completion of the surface mount process.

Mounting the PowerCap after the   surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers.

## CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the VS1743 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, bit 6 of the century register, see Table 2. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the VS1743 registers are updated simultaneously after the internal clock register updating process has been re-enabled. Updating is within a second after the read bit is written to 0.

The READ bit must be a zero for a minimum of 500µs to ensure the external registers will be updated.

## VS1743 BLOCK DIAGRAM Figure 1
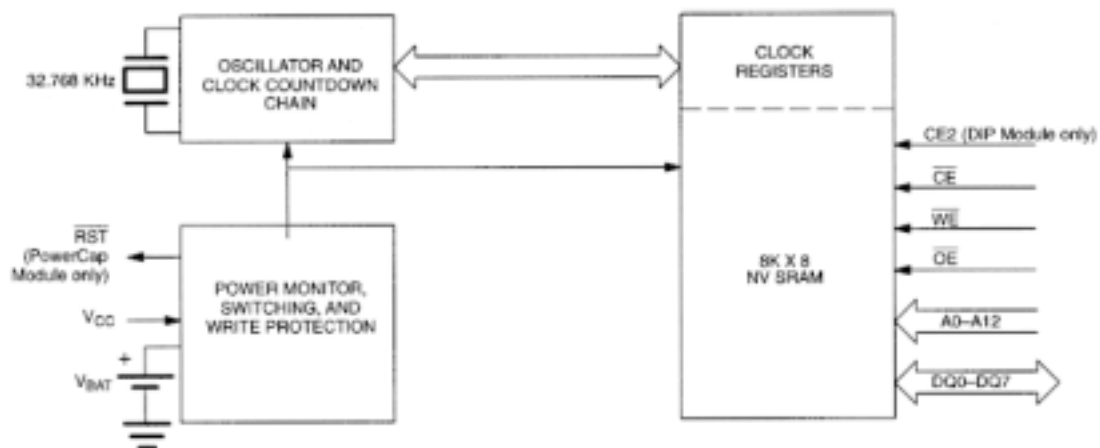


## VS1743 TRUTH TABLE Table 1

| $V_{CC}$ | $\overline{CE}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|---|
| $V_{CC} > V_{PF}$ | $V_{IH}$ | X | X | X | DESELECT | HIGH-Z | STANDBY |
| | X | $V_{IL}$ | X | X | DESELECT | HIGH-Z | STANDBY |
| | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | WRITE | DATA IN | ACTIVE |
| | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | READ | DATA OUT | ACTIVE |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | READ | HIGH-Z | ACTIVE |
| $V_{SO} < V_{CC} < V_{PF}$ | X | X | X | X | DESELECT | HIGH-Z | CMOS STANDBY |
| $V_{CC} < V_{SO} < V_{PF}$ | X | X | X | X | DESELECT | HIGH-Z | DATA RETENTION MODE |

## SETTING THE CLOCK

As shown in Table 2, bit 7 of the century register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the VS1743 registers. The user can then load them with the correct day, date and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB (bit 7) of the seconds registers, see Table 2. Setting it to a 1 stops the oscillator.

## FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, $\overline{WE}$ high, and address for seconds register remain valid and stable).

## CLOCK ACCURACY (DIP MODULE)

The VS1743 is guaranteed to keep time accuracy to within ±1 minute per month at 25℃. The RTC is calibrated at the factory using nonvolatile tuning elements, and does not require additional For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also effected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information please see application note 58.

## CLOCK ACCURACY (POWERCAP MODULE)

The VS1743 and PowerCap are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35 ppm) at 25°C. Clock accuracy is also effected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information please see application note 58.

## VS1743 REGISTER MAP Table 2

| ADDRESS | DATA | | | | | | | | FUNCTION/RANGE | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | B$_7$ | B$_6$ | B$_5$ | B$_4$ | B$_3$ | B$_2$ | B$_1$ | B$_0$ | | | |
| 1FFF | 10 Year | | | | YEAR | | | | YEAR | | 00-99 |
| 1FFE | X | X | X | 10 Mo | MONTH | | | | MONTH | | 01-12 |
| 1FFD | X | X | 10 Date | | DATE | | | | DATE | | 01-31 |
| 1FFC | BF | FT | X | X | X | DAY | | | DAY | | 01-07 |
| 1FFB | X | X | 10 HOUR | | HOUR | | | | HOUR | | 00-23 |
| 1FFA | X | 10 MINUTES | | | MINUTES | | | | MINUTES | | 00-59 |
| 1FF9 | $\overline{OSC}$ | 10 SECONDS | | | SECONDS | | | | SECONDS | | 00-59 |
| 1FF8 | W | R | 10 CENTURY | | CENTURY | | | | CONTROL | | 00-39 |

$\overline{OSC}$ = STOP BIT   R = READ BIT   FT = FREQUENCY TEST
W = WRITE BIT   X = SEE NOTE BELOW   BF = BATTERY FLAG

## NOTE:

All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

## RETRIEVING DATA FROM RAM OR CLOCK

The VS1743 is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t$_{AA}$ after the last address input is stable, providing that the $\overline{CE}$, and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$, or $\overline{OE}$ access times and states are not met, valid data will be available at the latter of chip enable access (t$_{CEA}$) or at output enable access time (t$_{CEA}$). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$, and $\overline{OE}$. If the outputs are activated before t$_{AA}$, the data lines are driven to an intermediate state until t$_{AA}$. If the address inputs are changed while $\overline{CE}$, and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t$_{OH}$) but will then go indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The VS1743 is in the write mode whenever $\overline{WE}$, and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$, on $\overline{CE}$. The

addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of $t_{WR}$ prior to the initiation of another read or write cycle. Data in must be valid $t_{DS}$ prior to the end of write and remain valid for $t_{DH}$ afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs $t_{WEZ}$ after $\overline{WE}$ goes active.

## DATA RETENTION MODE

The 5-volt device is fully accessible and data can be written or read only when $V_{CC}$ is greater than $V_{PF}$. However, when $V_{CC}$ is below the power fail point, $V_{PF}$, (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access.

At this time (PowerCap only)the power fail reset output signal ($\overline{RST}$) is driven active and will remain active until $V_{CC}$ returns to nominal levels. When $V_{CC}$ falls below the battery switch point $V_{SO}$ (battery supply level), device power is switched from the $V_{CC}$ pin to the backup battery. RTC operation and SRAM data are maintained from the battery until $V_{CC}$ is returned to nominal levels. The 3.3-volt device is fully accessible and data can be written or read only when $V_{CC}$ is greater than $V_{PF}$. When $V_{CC}$ falls below the power fail point, $V_{PF}$, access to the device is inhibited. At this time the power fail reset output signal ($\overline{RST}$) is driven active and will remain active until $V_{CC}$ returns to nominal levels. If $V_{PF}$ is less than $V_{SO}$, the device power is switched from $V_{CC}$ to the backup supply ($V_{BAT}$) when $V_{CC}$ drops below $V_{PF}$. If $V_{PF}$ is greater than $V_{SO}$, the device power is switched from $V_{CC}$ to the backup supply ($V_{BAT}$) when $V_{CC}$ drops below $V_{SO}$. RTC operation and SRAM data are maintained from the battery until $V_{CC}$ is returned to nominal levels. The $\overline{RST}$ (PowerCap only) signal is an open drain output and requires a pull up. Except for the $\overline{RST}$, all control, data, and address signals must be powered down when $V_{CC}$ is powered down.

## BATTERY LONGEVITY

The VS1743 has a lithium power source that is designed to provide energy for clock activity and clock and RAM data retention when the $V_{CC}$ supply is not present. The capability of this internal power supply is sufficient to power the VS1743 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25℃ with the internal clock oscillator running in the absence of $V_{CC}$ power. Each VS1743 is shipped with its lithium energy source disconnected, guaranteeing full energy

capacity. When $V_{CC}$ is first applied at a level greater than $V_{PF}$, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the
VS1743 will be much longer than 10 years since no lithium battery energy is consumed when $V_{CC}$ is present.

## BATTERY MONITOR

The VS1743 constantly monitors the battery voltage of the internal battery. The Battery Flag bit (bit 7) of the day register is used to indicate the voltage level range of the battery. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC and RAM are questionable.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | -0.3V to +6.0V |
| Operating Temperature | 0℃ to 70℃ |
| Storage Temperature | -40℃ to +85℃ |
| Soldering Temperature | See J-STD-020A Specification (See Note 8) |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## OPERATING RANGE

| Range | Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 10% or 5V ± 10% |

## RECOMMENDED DC OPERATING CONDITIONS

(Over the Operating Range)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 Voltage All Inputs | | | | | | |
| $V_{CC}$ = 5V ±10% | $V_{IH}$ | 2.2 | | $V_{CC}$ +0.3V | V | 1 |
| $V_{CC}$ = 3.3V ±10% | $V_{IH}$ | 2.0 | | $V_{CC}$ +0.3V | V | 1 |
| Logic 0 Voltage All Inputs | | | | | | |
| $V_{CC}$ = 5V ±10% | $V_{IL}$ | -0.3 | | 0.8 | V | 1 |
| $V_{CC}$ = 3.3V ±10% | $V_{IL}$ | -0.3 | | 0.6 | V | 1 |

## DC ELECTRICAL CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Active Supply Current | $I_{CC}$ | | 15 | 50 | mA | 2, 3 |
| TTL Standby Current ($\overline{CE} = V_{IH}$, CE2=$V_{IL}$) | $I_{CC1}$ | | 1 | 3 | mA | 2, 3 |
| CMOS Standby Current ($\overline{CE} \geq V_{CC} - 0.2V$, CE2= GND + 0.2V) | $I_{CC2}$ | | 1 | 3 | mA | 2, 3 |
| Input Leakage Current (any input) | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current (any output) | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT} = -1.0$ mA) | $V_{OH}$ | 2.4 | | | | 1 |
| Output Logic 0 Voltage ($I_{OUT} = 2.1$ mA) | $V_{OL1}$ | | | 0.4 | | 1 |
| Write Protection Voltage | $V_{PF}$ | 4.25 | | 4.50 | V | 1 |
| Battery Switch-over Voltage | $V_{SO}$ | | $V_{BAT}$ | | | 1, 4 |

## DC ELECTRICAL CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 3.3V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Active Supply Current | $I_{CC}$ | | 10 | 30 | mA | 2, 3 |
| TTL Standby Current ($\overline{CE} = V_{IH}$) | $I_{CC1}$ | | 0.7 | 2 | mA | 2, 3 |
| CMOS Standby Current ($\overline{CE} \geq V_{CC} - 0.2V$, CE2 = GND + 0.2V) | $I_{CC2}$ | | 0.7 | 2 | mA | 2, 3 |
| Input Leakage Current (any input) | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current (any output) | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT} = -1.0$ mA) | $V_{OH}$ | 2.4 | | | | 1 |
| Output Logic 0 Voltage ($I_{OUT} = 2.1$ mA) | $V_{OL1}$ | | | 0.4 | | 1 |
| Write Protection Voltage | $V_{PF}$ | 2.80 | | 2.97 | V | 1 |
| Battery Switch-over Voltage | $V_{SO}$ | | $V_{BAT}$ or $V_{PF}$ | | V | 1, 4 |

## READ CYCLE, AC CHARACTERISTICS

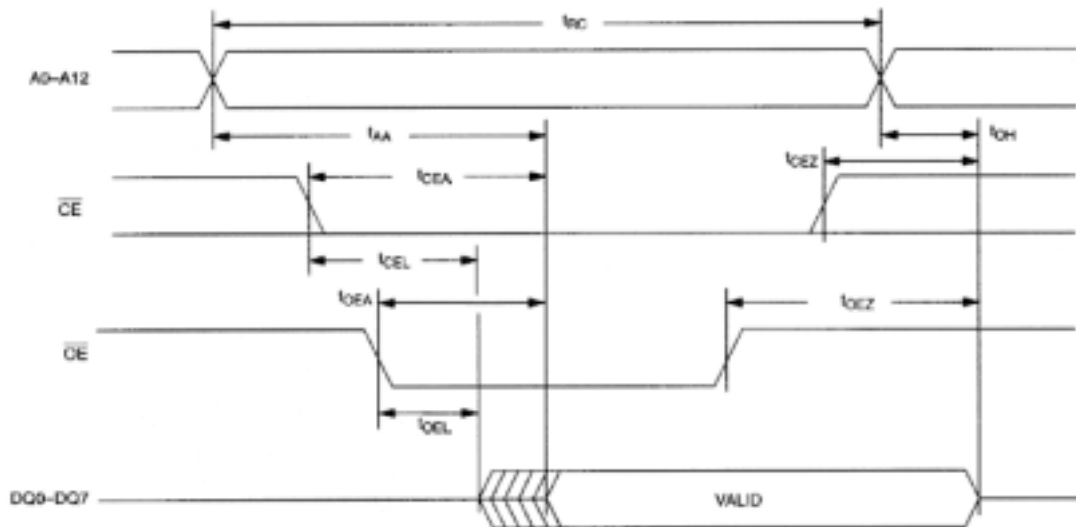(Over the Operating Range; $V_{CC}$ = 5.0V ± 10%)

| PARAMETER | SYMBOL | 70 ns access | | 100 ns access | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Read Cycle Time | $t_{RC}$ | 70 | | 100 | | ns | 5 |
| Address Access Time | $t_{AA}$ | | 70 | | 100 | ns | 5 |
| $\overline{CE}$ to CE2 to DQ Low-Z | $t_{CEL}$ | 5 | | 5 | | ns | 5 |
| $\overline{CE}$ Access Time | $t_{CEA}$ | | 70 | | 100 | ns | 5 |
| CE2 Access Time | $t_{CE2A}$ | | 80 | | 105 | ns | 5 |
| $\overline{CE}$ and CE2 Data Off time | $t_{CEZ}$ | | 25 | | 35 | ns | 5 |
| $\overline{OE}$ to DQ Low-Z | $t_{OEL}$ | 5 | | 5 | | ns | 5 |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | 35 | | 55 | ns | 5 |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | 25 | | 35 | ns | 5 |
| Output Hold from Address | $t_{OH}$ | 5 | | 5 | | ns | 5 |

## READ CYCLE, AC CHARACTERISTICS

(Over the Operating Range; $V_{CC}$ = 3.3V ± 10%)

| PARAMETER | SYMBOL | 120 ns access | | 150 ns access | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | ns | 5 |
| Address Access Time | $t_{AA}$ | | 120 | | 150 | ns | 5 |
| $\overline{CE}$ and CE2 Low to DQ Low-Z | $t_{CEL}$ | 5 | | 5 | | ns | 5 |
| $\overline{CE}$ and CE2 Access Time | $t_{CEA}$ | | 120 | | 150 | ns | 5 |
| $\overline{CE}$ and CE2 Data Off time | $t_{CEZ}$ | | 40 | | 50 | ns | 5 |
| $\overline{OE}$ Low to DQ Low-Z | $t_{OEL}$ | 5 | | 5 | | ns | 5 |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | 100 | | 130 | ns | 5 |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | 35 | | 35 | ns | 5 |
| Output Hold from Address | $t_{OH}$ | 5 | | 5 | | ns | 5 |

## READ CYCLE TIMING DIAGRAM



SEE NOTES

## WRITE CYCLE, AC CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER | SYMBOL | 70 ns access MIN | MAX | 100 ns access MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 70 | | 100 | | ns | 5 |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns | 5 |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 50 | | 70 | | ns | 5 |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 60 | | 75 | | ns | 5 |
| CE2 Pulse Width | $t_{CE2W}$ | 65 | 85 | | | ns | 5 |
| Data Setup Time | $t_{DS}$ | 30 | | 40 | | ns | 5 |
| Data Hold time | $t_{DH}$ | 0 | | 0 | | ns | 5 |
| Address Hold Time | $t_{AH}$ | 5 | | 5 | | ns | 5 |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | 25 | | 35 | ns | 5 |
| Write Recovery Time | $t_{WR}$ | 5 | | 5 | | ns | 5 |

## WRITE CYCLE, AC CHARACTERISTICS

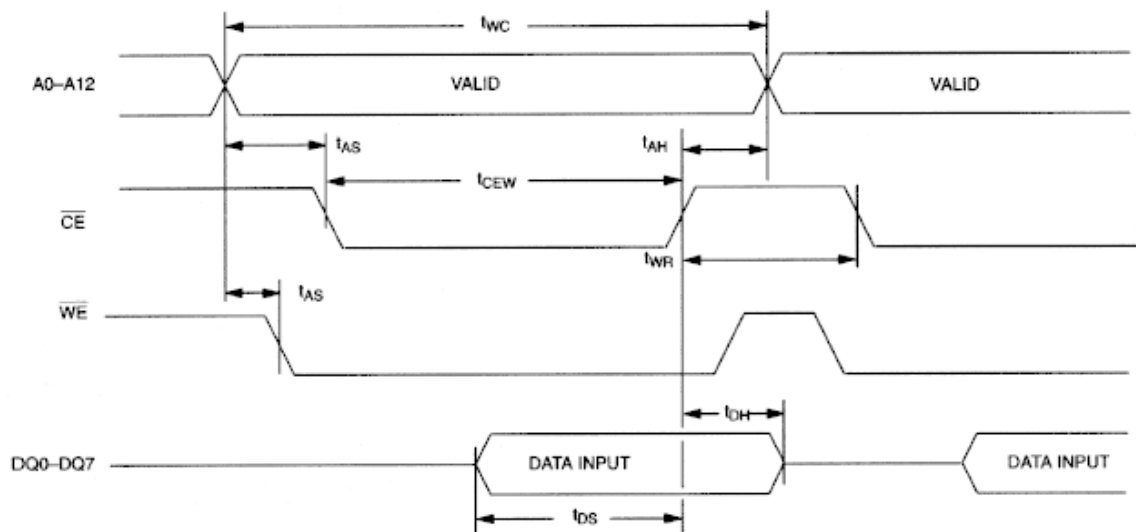(Over the Operating Range; $V_{CC} = 3.3V \pm 10\%$)

| PARAMETER | SYMBOL | 120 ns access | | 150 ns access | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | ns | 5 |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns | 5 |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 100 | | 130 | | ns | 5 |
| $\overline{CE}$ and CE2 Pulse Width | $t_{CEW}$ | 110 | | 140 | | ns | 5 |
| Data Setup Time | $t_{DS}$ | 80 | | 90 | | ns | 5 |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | ns | 5 |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | ns | 5 |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | 40 | | 50 | ns | 5 |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | ns | 5 |

## WRITE CYCLE TIMING, WRITE ENABLE CONTROLLED

(SEE NOTE 5)
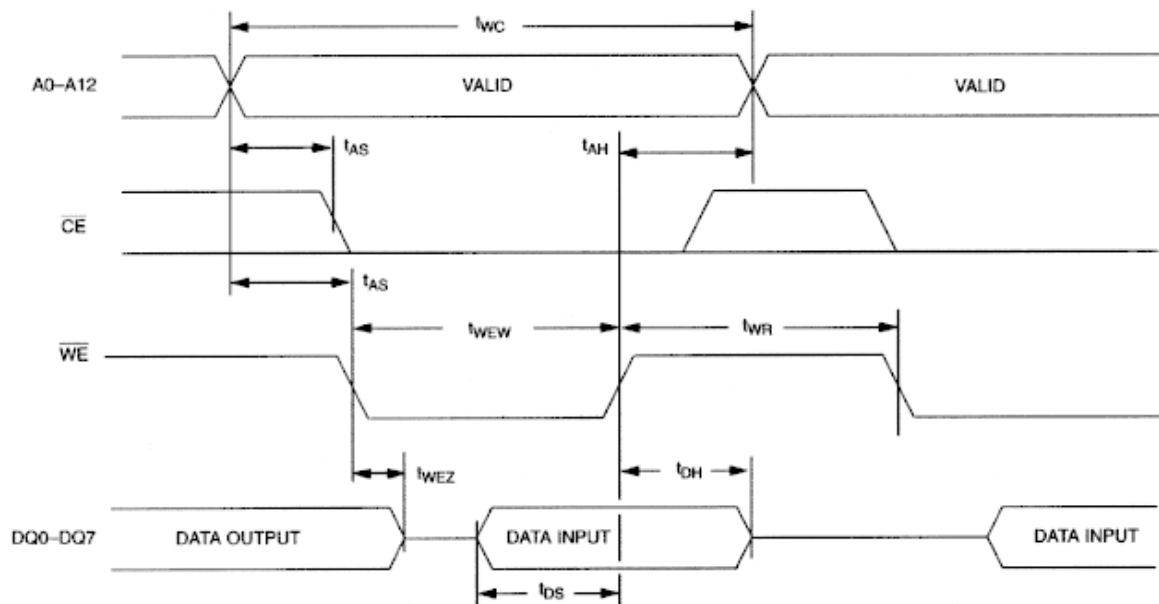
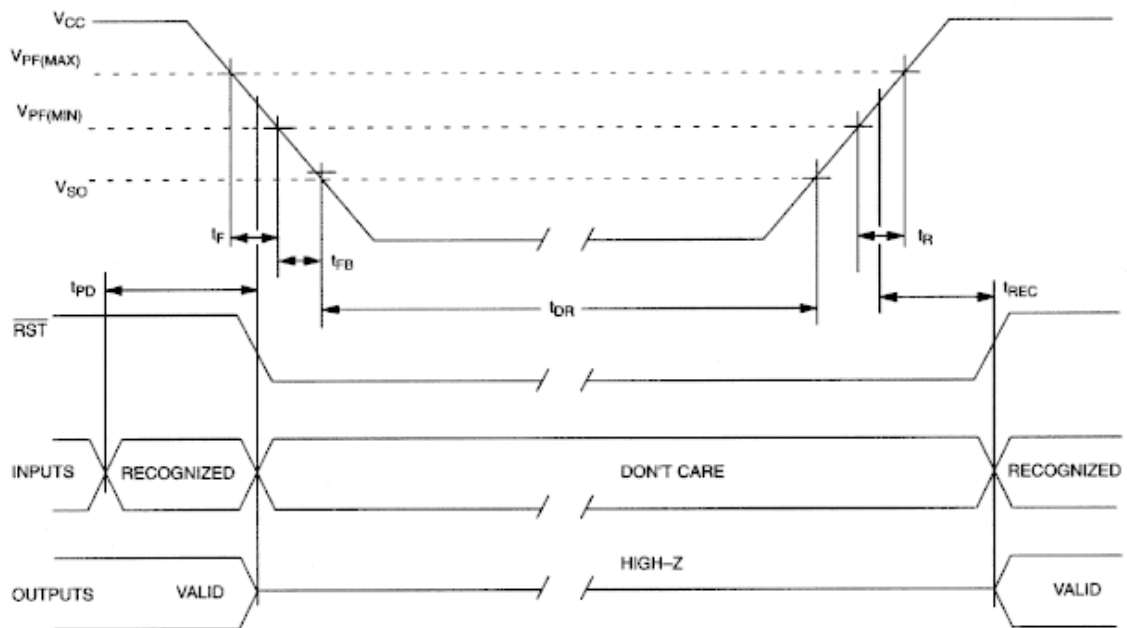## WRITE CYCLE TIMING, $\overline{CE}$, CE2 CONTROLLED    (SEE NOTE 5)



## POWER-UP/DOWN CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 5.0V \pm 10\%$)

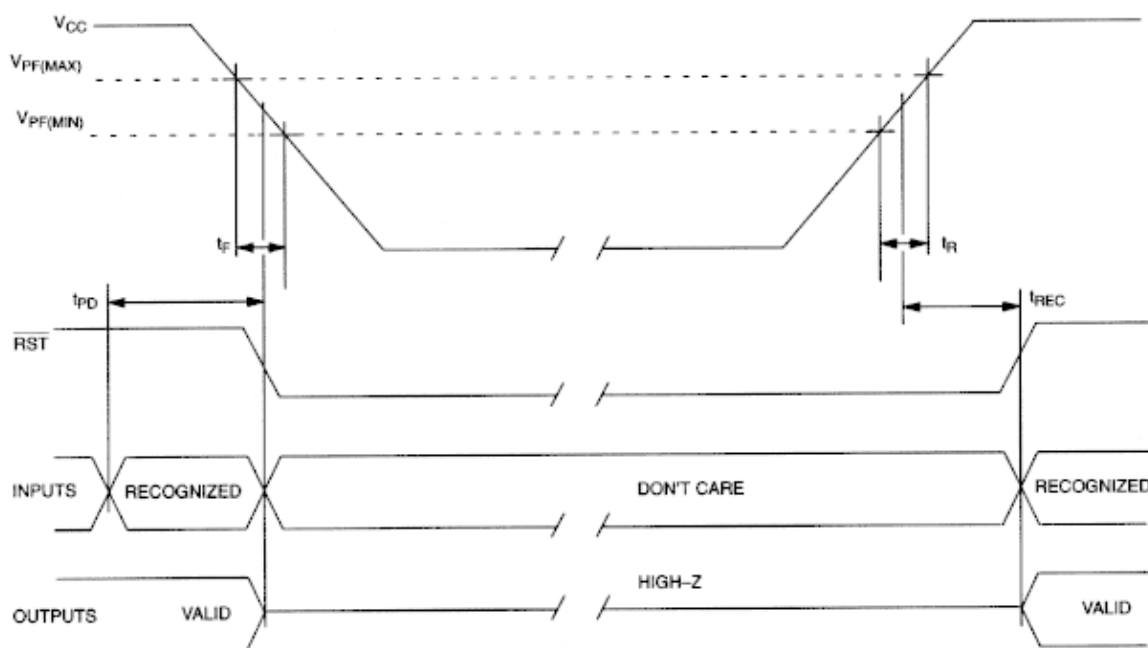| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$, CE2 at $V_{IL}$, Before Power-Down | $t_{PD}$ | 0 | | | μs | |
| $V_{CC}$ Fall Time: $V_{PF}$(MAX) to $V_{PF}$(Min) | $t_F$ | 300 | | | μs | |
| $V_{CC}$ Fall Time: $V_{PF}$(MIN) to $V_{SO}$ | $t_{FB}$ | 10 | | | μs | |
| $V_{CC}$ Rise Time: $V_{PF}$(MIN) to $V_{PF}$(MAX) | $t_R$ | 0 | | | μs | |
| Power-up Recover Time | $t_{REC}$ | | | 35 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 6, 7 |

## POWER-UP/POWER-DOWN TIMING 5-VOLT DEVICE



## POWER-UP/DOWN CHARACTERISTICS

(Over the Operating Range; $V_{CC}$ = 3.3V $\pm$ 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$, Before Power-Down | $t_{PD}$ | 0 | | | µs | |
| $V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(Min)}$ | $t_F$ | 300 | | | µs | |
| $V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$ | $t_R$ | 0 | | | µs | |
| $V_{PF}$ to $\overline{RST}$ High | $t_{REC}$ | | | 35 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 6, 7 |

## POWER-UP/DOWN WAVEFORM TIMING 3.3-VOLT DEVICE



## CAPACITANCE ($t_A = 25°C$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Capacitance on all input pins | $C_{IN}$ | | | 7 | pF | |
| Capacitance on all output pins | $C_O$ | | | 10 | pF | |

## AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0.0 to 3.0V

Timing Measurement Reference Levels:
        Input: 1.5V
        Output: 1.5V
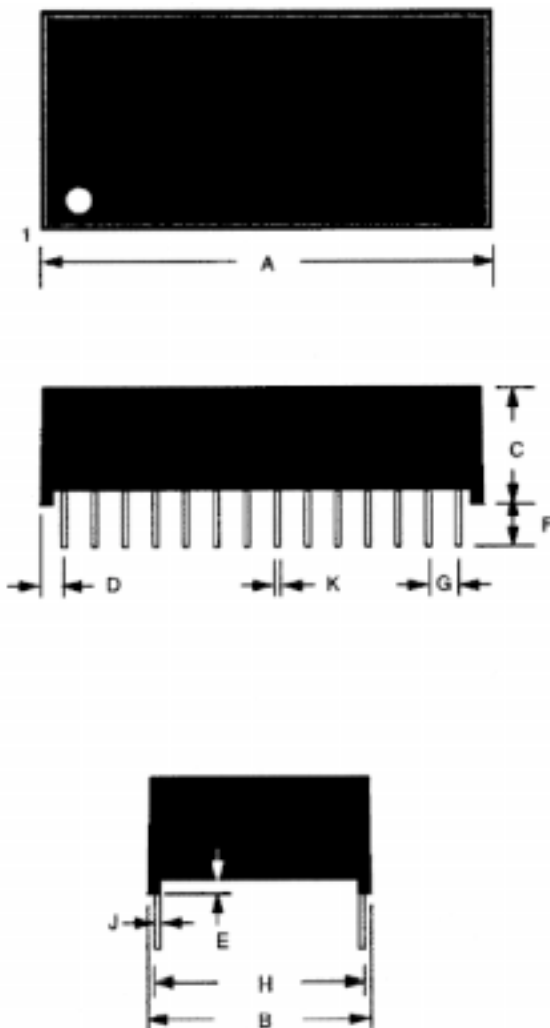Input Pulse Rise and Fall Times: 5 ns

## NOTES:

1. Voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Battery switchover occurs at the lower of either the battery terminal voltage or $V_{PF}$.

5. The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the

    logic levels for active and inactive levels are opposite.
6. Data retention time is at 25°C.

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7. Each VS1743 has a built-in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected t $_{DR}$ is defined for DIP modules as a cumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.

8. Real-Time Clock Modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85℃. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.
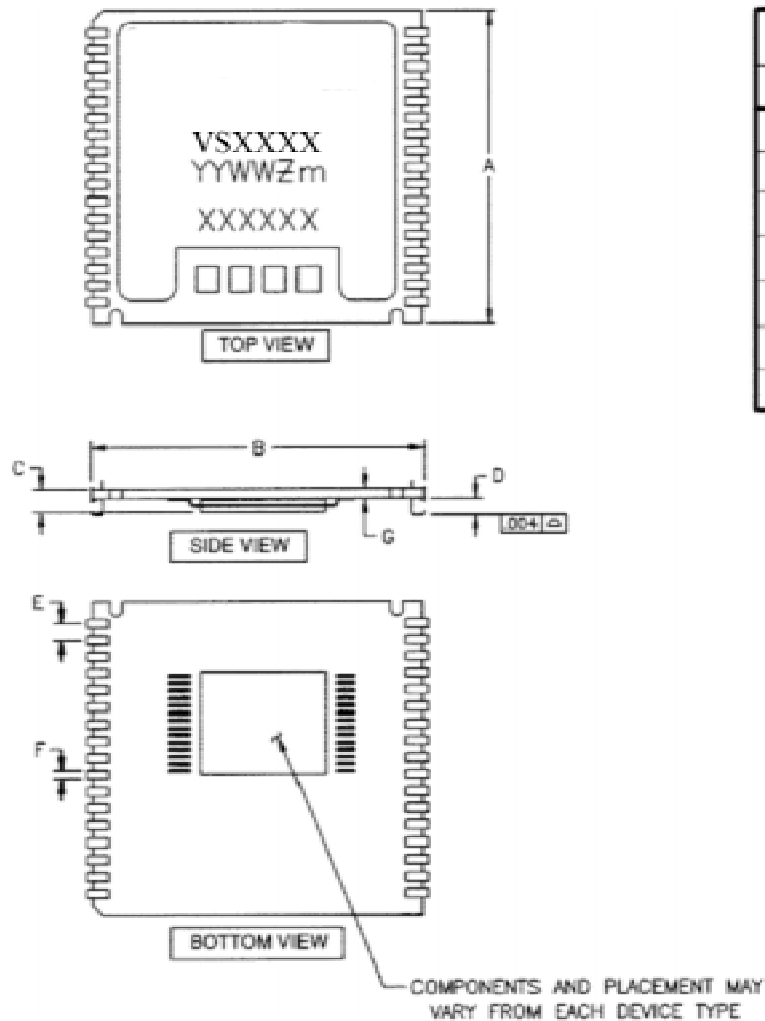
In addition, for the PowerCap:

    a. Recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up ("live - bug").

    b. Hand Soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 (three) seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflow and use a solder wick to remove solder.

## VS1743 28-PIN PACKAGE



| PKG | 28–PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A IN. | 1.470 | 1.490 |
| MM | 37.34 | 37.85 |
| B IN. | 0.675 | 0.740 |
| MM | 17.75 | 18.80 |
| C IN. | 0.315 | 0.335 |
| MM | 8.51 | 9.02 |
| D IN. | 0.075 | 0.105 |
| MM | 1.91 | 2.67 |
| E IN. | 0.015 | 0.030 |
| MM | 0.38 | 0.76 |
| F IN. | 0.140 | 0.180 |
| MM | 3.56 | 4.57 |
| G IN. | 0.090 | 0.110 |
| MM | 2.29 | 2.79 |
| H IN. | 0.590 | 0.630 |
| MM | 14.99 | 16.00 |
| J IN. | 0.010 | 0.018 |
| MM | 0.25 | 0.45 |
| K IN. | 0.015 | 0.025 |
| MM | 0.43 | 0.58 |

## VS1743P



| PKG | INCHES | | |
|-----|-----|-----|-----|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.980 | 0.985 | 0.990 |
| C | – | – | 0.080 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.025 | 0.027 | 0.030 |

TOP VIEW

SIDE VIEW

BOTTOM VIEW

COMPONENTS AND PLACEMENT MAY VARY FROM EACH DEVICE TYPE.

## NOTE:

Recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up ("live-bug").

Hand Soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 (three) seconds.

To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.
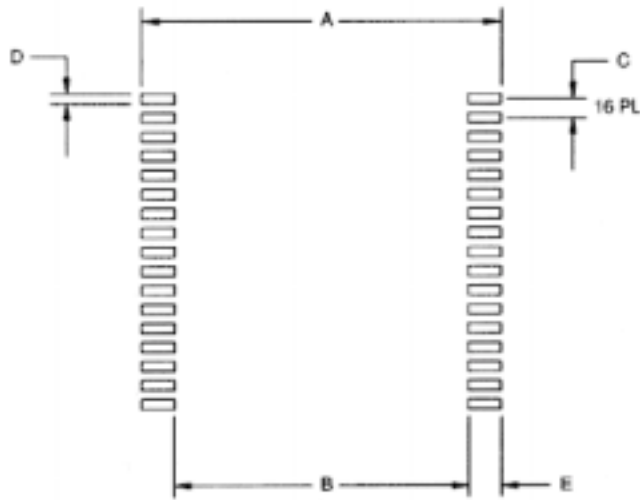
## VS1743P WITH PowerCap ATTACHED
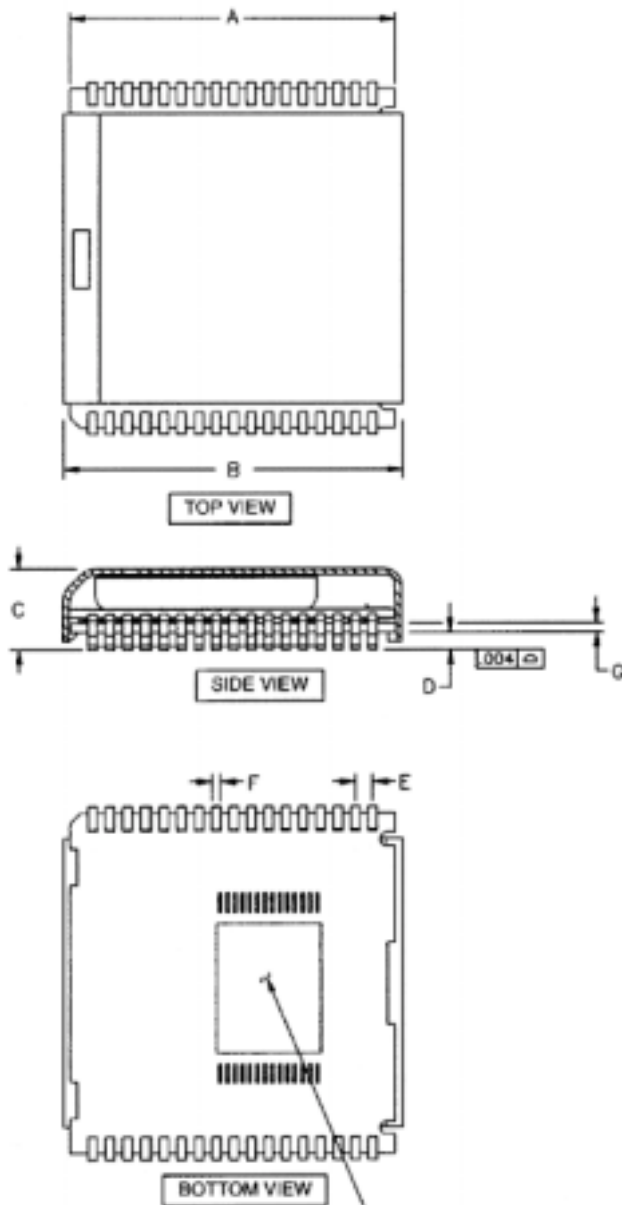


| PKG | INCHES | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.955 | 0.960 | 0.965 |
| C | 0.240 | 0.245 | 0.250 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.020 | 0.025 | 0.030 |

TOP VIEW

SIDE VIEW

BOTTOM VIEW

— COMPONENTS AND PLACEMENT MAY VARY FROM EACH DEVICE TYPE

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## RECOMMENDED POWERCAP MODULE LAND PATTERN



| PKG DIM | INCHES | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | – | 1.050 | – |
| B | – | 0.826 | – |
| C | – | 0.050 | – |
| D | – | 0.030 | – |
| E | – | 0.112 | – |