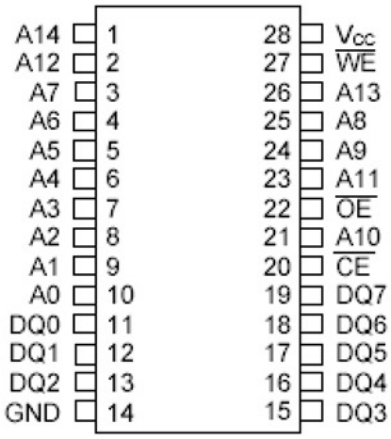
VS1744

Y2KC Nonvolatile Timekeeping

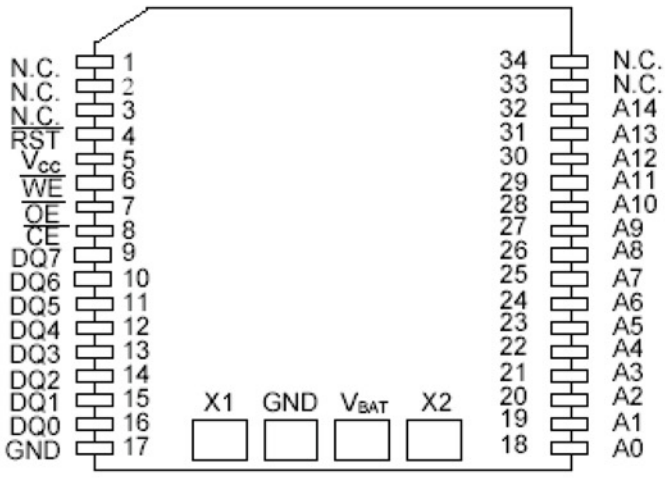
FEATURES

- Integrated NV SRAM, real-time clock, crystal, power-fail control circuit, and lithium energy source
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Century byte register; Y2K-compliant
- Totally nonvolatile with over 10 years of operation in the absence of power
- BCD-coded century, year, month, date, day, hours, minutes, and seconds with automatic leap-year compensation valid up to the year 2100
- Battery voltage-level indicator flag
- Power-fail write protection allows for ±10% V_{CC} power-supply tolerance
- Lithium energy source is electrically _disconnected to retain freshness until power is applied for the first time
- DIP module only
  _Standard JEDEC byte-wide 32k x 8 static RAM pinout
- PowerCap® module board only
  _Surface-mountable package for direct connection to PowerCap containing battery and crystal
  _Replaceable battery (PowerCap)
  _Power-on reset output
- Available in industrial temperature range: -40°C to +85°C

PIN ASSIGNMENT (Top View)



28-Pin Module PDIP
(700mil Extended)



34-Pin PowerCap Module Board

ORDERING INFORMATION

PART	PIN-PACKAGE	VOLTAGE (V)	TEMP RANGE	TOP MARK
VS1744-70	28 PDIP Module	5	0°C to +70°C	VS1744-70
VS1744-70IND	28 PDIP Module	5	-40°C to +85°C	VS1744-70IND
VS1744P-70	34 PowerCap*	5	0°C to +70°C	VS1744P-70
VS1744P-70IND	34 PowerCap*	5	-40°C to +85°C	VS1744P-70IND
VS1744W-120	28 DIP Module	3.3	0°C to +70°C	VS1744W-120
VS1744W-120IND	28 DIP Module	3.3	-40°C to +85°C	VS1744W-120IND
VS1744WP-120	34 PowerCap*	3.3	0°C to +70°C	VS1744WP-120
VS1744WP-120IND	34 PowerCap*	3.3	-40°C to +85°C	VS1744WP-120IND

PIN DESCRIPTION

A0–A14 - Address Input

$\overline{CE}$ ` - Chip Enable

$\overline{OE}$ - Output Enable

$\overline{WE}$ - Write Enable

V_{CC} - Power-Supply Input
GND - Ground
DQ0–DQ - Data Input/Output
N.C. - No Connection

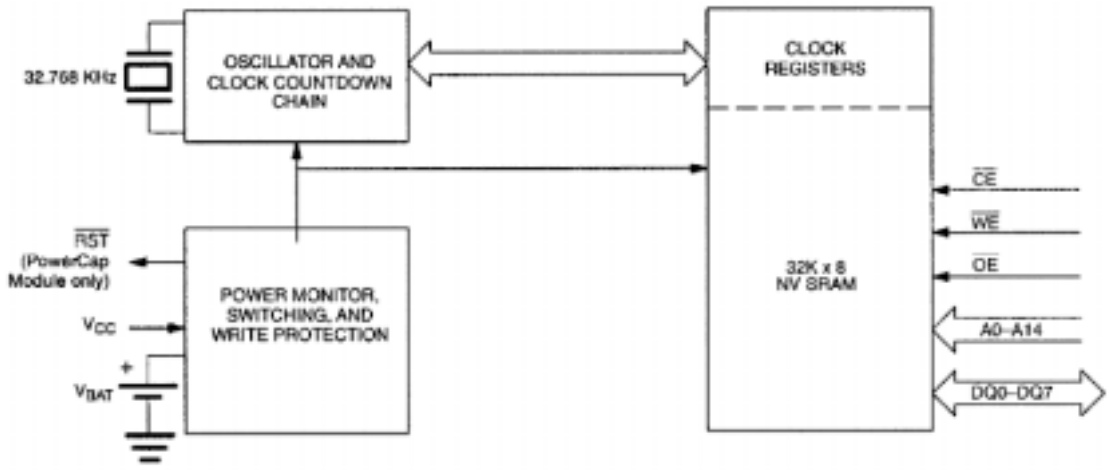
$\overline{RST}$ - Power-On Reset Output (PowerCap module board only)

X1, X2 - Crystal Connection
V_{BAT} - Battery Connection

DESCRIPTION

The VS1744 is a full function, year 2000 compliant (Y2KC), real-time clock/calendar (RTC) and 32k x 8 NV SRAM. User access to all registers within the VS1744 is accomplished with a byte-wide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the date of each month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The VS1744 also contains its own power-fail circuitry that deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

Figure 1. BLOCK DIAGRAM



PACKAGES

The VS1744 is available in two packages (28-pin DIP and 34-pin PowerCap module). The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap module board is designed with contacts for connection to a separate PowerCap that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the VS1744P after the completion of the surface-mount process. Mounting the PowerCap after the surface-mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap module board and PowerCap are ordered separately and shipped in separate containers.

CLOCK OPERATIONS: READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the VS1744 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, bit 6 of the century register (Table 2). As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is, day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the VS1744 registers are updated simultaneously after the internal clock-register updating process has been re-enabled. Updating is within a second after the read bit is written to 0. The READ bit must be a 0 for a minimal of 500µs to ensure the external registers are updated.

Table 1. VS1744 TRUTH TABLE

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
$V_{CC} > V_{PF}$	V_{IH}	X	X	DESELECT	HIGH-Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH-Z	ACTIVE
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	DESELECT	HIGH-Z	CMOS STANDBY
$V_{CC} < V_{SO} < V_{PF}$	X	X	X	DESELECT	HIGH-Z	DATA RETENTION MODE

SETTING THE CLOCK

As shown in Table 2, bit 7 of the century register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the VS1744 registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator can be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB (bit 7) of the seconds registers (Table2). Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register toggles at 512Hz. When the seconds register is being read, the DQ0 line toggles at the 512Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, $\overline{WE}$ high, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The VS1744 is guaranteed to keep time accuracy to within ±1 minute per month at +25℃. The RTC is calibrated at the factory using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also affected by the electrical environment; caution should be taken to place the RTC in the lowest level EMI section of the PC board layout

CLOCK ACCURACY (POWERCAP MODULE)

The VS1744 individually tested for accuracy. Once mounted together, the module typically keeps

time accuracy to within ±1.53 minutes per month (35ppm) at +25°C. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PC board layout.

Table 2. VS1744 REGISTER MAP

ADDRESS	DATA								FUNCTION/RANGE	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FFF	10 YEAR				YEAR				YEAR	00-99
7FFE	X	X	X	10 MO	MONTH				MONTH	01-12
7FFD	X	X	10 DATE		DATE				DATE	01-31
7FFC	BF	FT	X	X	X	DAY			DAY	01-07
7FFB	X	X	10 HOUR		HOUR				HOUR	00-23
7FFA	X	10 MINUTES			MINUTES				MINUTES	00-59
7FF9	$\overline{OSC}$	10 SECONDS			SECONDS				SECONDS	00-59
7FF8	W	R	10 CENTURY		CENTURY				CENTURY	00-39

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = SEE NOTE BF = BATTERY FLAG

Note: All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The VS1744 is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data is available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times and states are not met, valid data is available at the latter of chip-enable access (t_{CEA}) or at output-enable access time (t_{OEA}). The state of the DQ pins is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data remains valid for output-data hold time (t_{OH}) but then goes indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The VS1744 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held

valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal is high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low, the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ then disables the output t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

The 5V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF} . However, when V_{CC} is below the power-fail point, V_{PF} (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. At this time the power-fail reset-output signal ($\overline{RST}$) is driven active and remains active until V_{CC} returns to nominal levels. When V_{CC} falls below the battery switch point V_{SO} (battery supply level), device power is switched from the V_{CC} pin to the backup battery. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. The 3.3V device is fully accessible, and data can be written or read only when V_{CC} is greater than V_{PF} . When V_{CC} falls below V_{PF} access to the device is inhibited. At this time the power-fail reset-output signal ($\overline{RST}$) is driven active and remains active until V_{CC} returns to nominal levels. If V_{PF} is less than V_{SO}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{PF} . If V_{PF} is greater than V_{SO}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{SO}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. The $\overline{RST}$ signal is an open-drain output and requires a pullup. Except for the $\overline{RST}$, all control, data, and address signals must be powered down when V_{CC} is powered down.

BATTERY LONGEVITY

The VS1744 has a lithium power source that is designed to provide energy for clock activity and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the VS1744 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25℃ with the internal clock oscillator running in the absence of V_{CC} power. Each VS1744 is shipped with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at

a level greater than V_{PF}, the lithium energy source is enabled for battery-backup operation. Actual life expectancy of the VS1744 is much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

BATTERY MONITOR

The VS1744 constantly monitors the battery voltage of the internal battery. The battery flag bit (bit 7) of the day register is used to indicate the voltage-level range of the battery. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated, and both the contents of the RTC and RAM are questionable.

ABSOLUTE MAXIMUM RATINGS *

Voltage Range on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Soldering Temperature	See IPC/JEDEC J-STD-020A (DIP Package) (Note 7)

*This is a stress rating only and functional operation of the device at these or any other condition beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

OPERATING RANGE

RANGE	TEMP RANGE	V_{CC}
Commercial	0°C to +70°C	3.3V ±10% or 5V ±10%
Industrial	-40°C to +85°C	3.3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS (Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage (All Inputs) V_{CC} = 5V ±10%	V_{IH}	2.2		V_{CC} + 0.3V	V	1
V_{CC} = 3.3V ±10%	V_{IH}	2.0		V_{CC} + 0.3V	V	
Logic 0 Voltage (All Inputs) V_{CC} = 5V ±10%	V_{IL}	-0.3		0.8	V	
V_{CC} = 3.3V ±10%	V_{IL}	0.3		0.6	V	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}			75	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			6	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)	Icc_2			4	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25		4.50	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT}			1, 4

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}			30	mA	2,3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			2	mA	2,3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)	I_{CC2}			2	mA	2,3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	2.80		2.97	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	1,4

READ CYCLE, AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, Over the operating range)

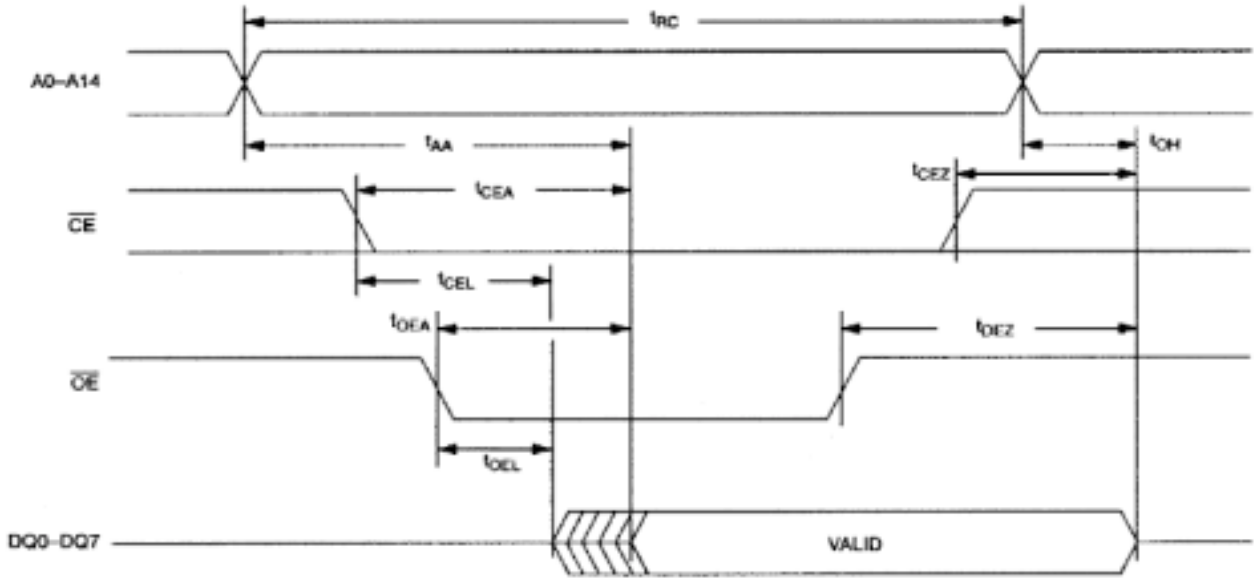
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70			ns	
Address Access Time	t_{AA}			70	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ Access Time	t_{CEA}			70	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			25	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			35	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			25	ns	
Output Hold from Address	t_{OH}	5			ns	

READ CYCLE, AC CHARACTERISTICS

(V_{CC} = 3.3V ±10%, Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			100	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			35	ns	
Output Hold from Address	t_{OH}	5			ns	

READ CYCLE TIMING DIAGRAM



WRITE CYCLE, AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, Over the operating range)

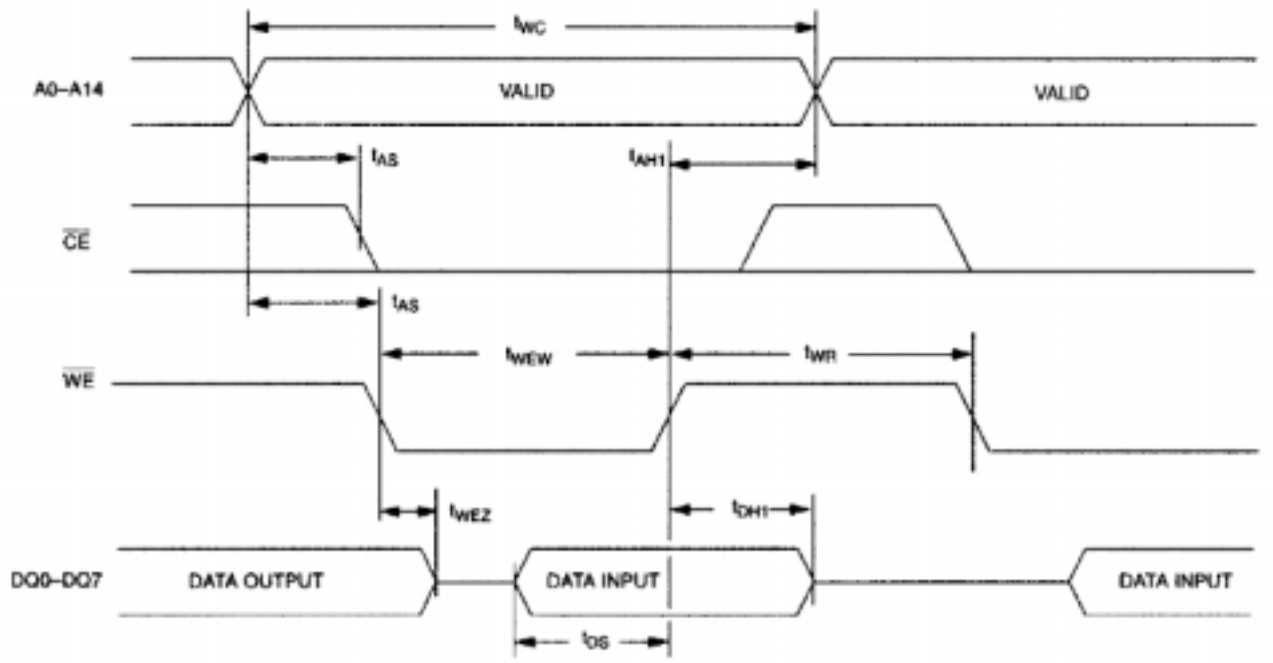
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	70			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60			ns	
Data Setup Time	t_{DS}	30			ns	
Data Hold Time	t_{DH1}	0			ns	8
Data Hold Time	t_{DH2}	0			ns	9
Address Hold Time	t_{AH1}	5			ns	8
Address Hold Time	t_{AH2}	5			ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}			25	ns	
Write Recovery Time	t_{WR}	5			ns	

WRITE CYCLE, AC CHARACTERISTICS

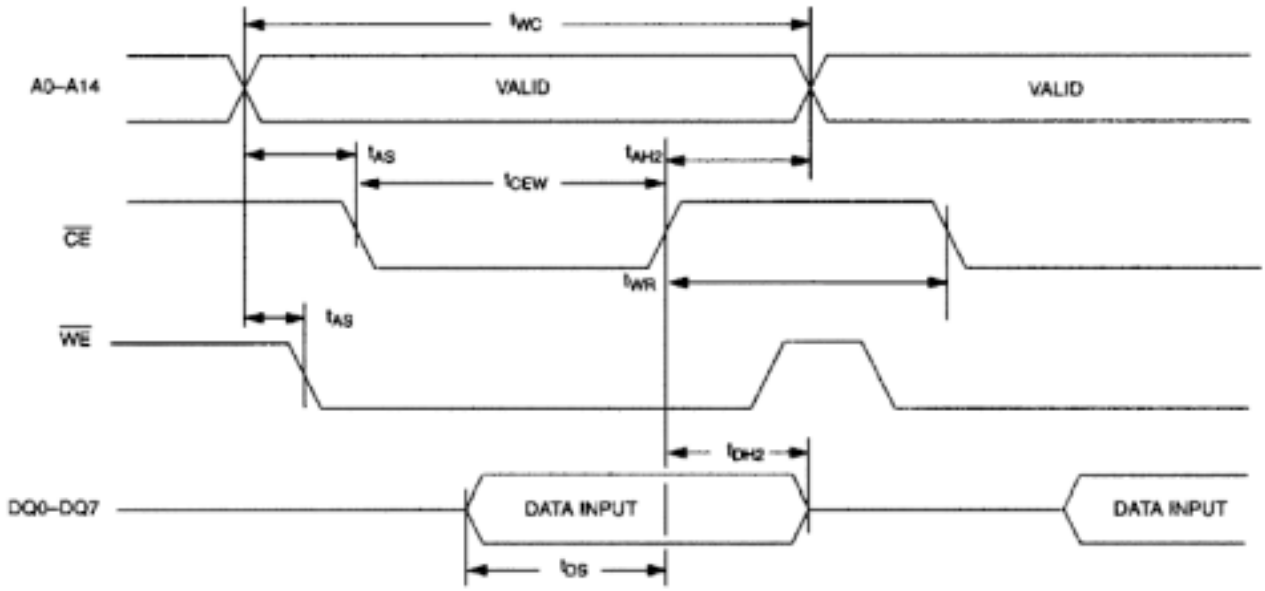
(V_{CC} = 3.3V ±10%, Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AS}	0		120	ns	
$\overline{WE}$ Pulse Width	t_{WEW}	100			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	110			ns	
$\overline{CE}$ and CE2 Pulse Width	t_{CEW}	110			ns	
Data Setup Time	t_{DS}	80			ns	
Data Hold Time	t_{DH1}	0			ns	8
Data Hold Time	t_{DH2}	0			ns	9
Address Hold Time	t_{AH1}	0			ns	8
Address Hold Time	t_{AH2}	10			ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
Write Recovery Time	t_{WR}	10			ns	

WRITE CYCLE TIMING DIAGRAM, WRITE-ENABLE CONTROLLED



WRITE CYCLE TIMING DIAGRAM, CHIP-ENABLE CONTROLLED

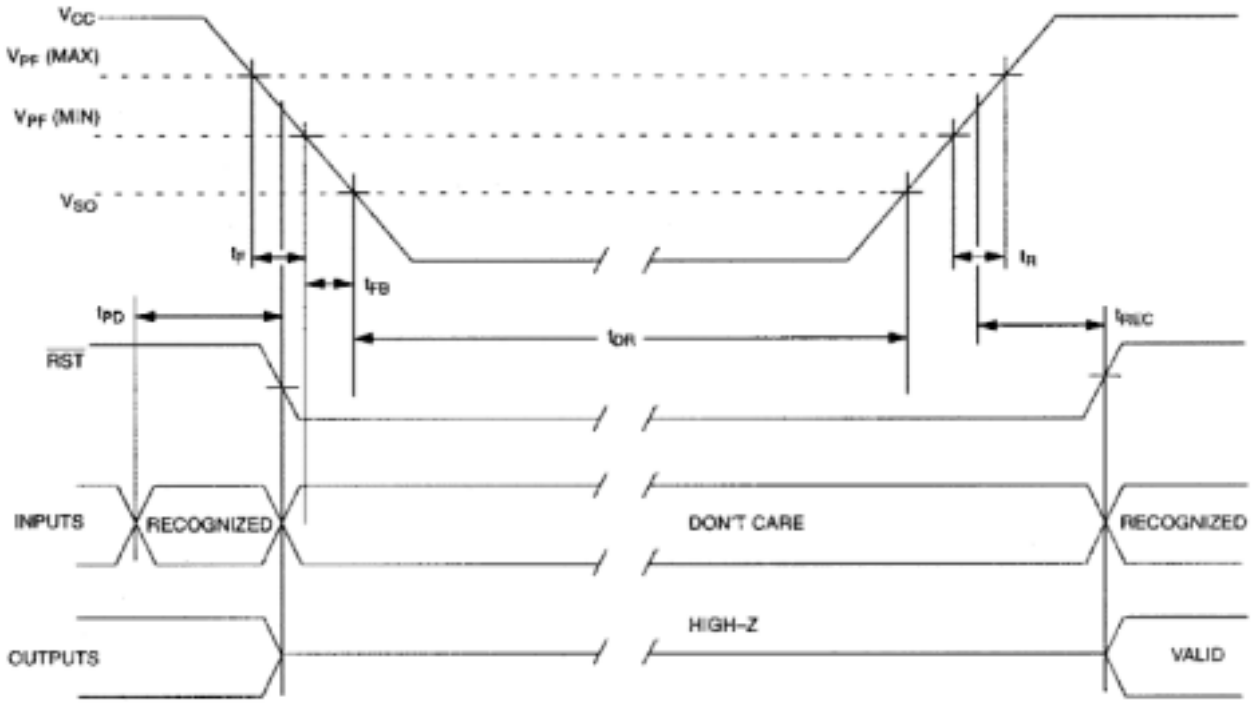


POWER-UP/DOWN AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator ON)	t_{DR}	10			years	5, 6

POWER-UP/DOWN TIMING, 5V

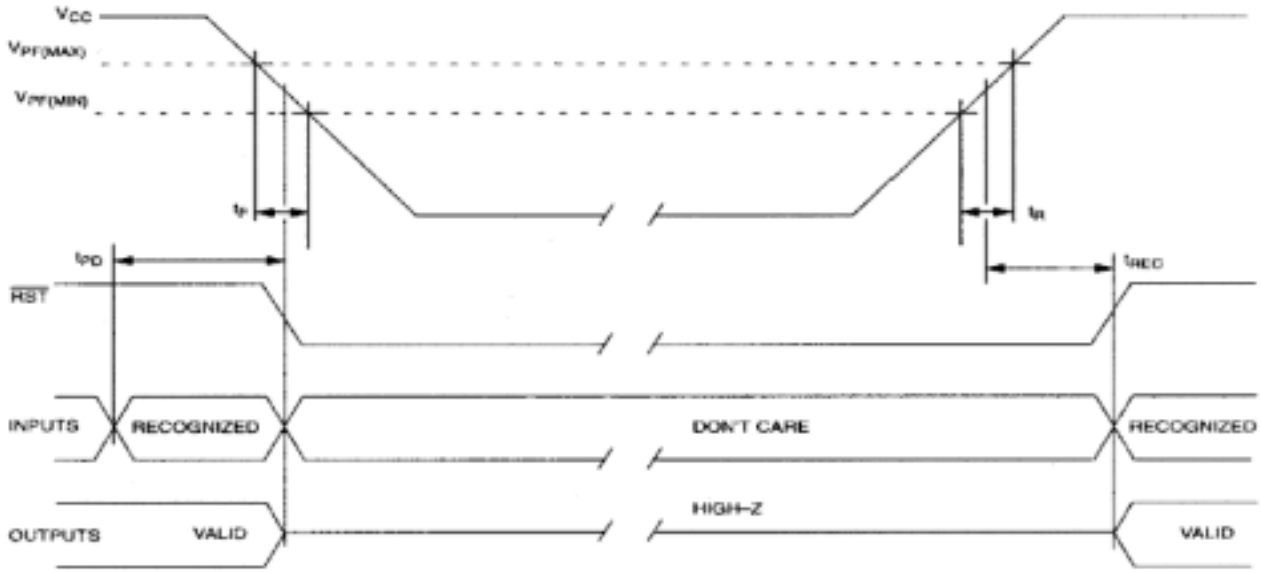


POWER-UP/DOWN CHARACTERISTICS

(V_{CC} = 3.3V ±10%, Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator ON)	t_{DR}	10			years	5, 6

POWER-UP/DOWN WAVEFORM TIMING, 3.3V



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance On All Input Pins	C_{IN}			7	pF	
Capacitance On All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0V to 3.0V

Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switchover occurs at the lower of either the battery terminal voltage or V_{PF} .
5) Data retention time is at +25°C.
6) Each VS1744 has a built-in switch that disconnects the lithium source until the user first applies V_{CC}. The expected t_{DR} is defined for DIP modules and assembled PowerCap modules as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

7) RTC modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used.

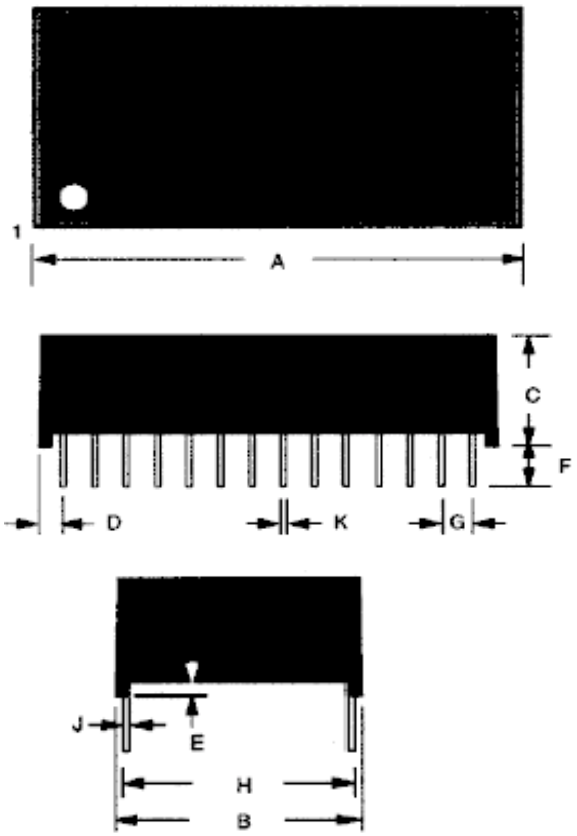
   In addition, for the PowerCap:

   a. recommends that PowerCap module bases experience one passthrough solder reflow oriented with the label side up (“live-bug”).
   b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad, and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows, and use a solder wick to remove solder.

8) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.

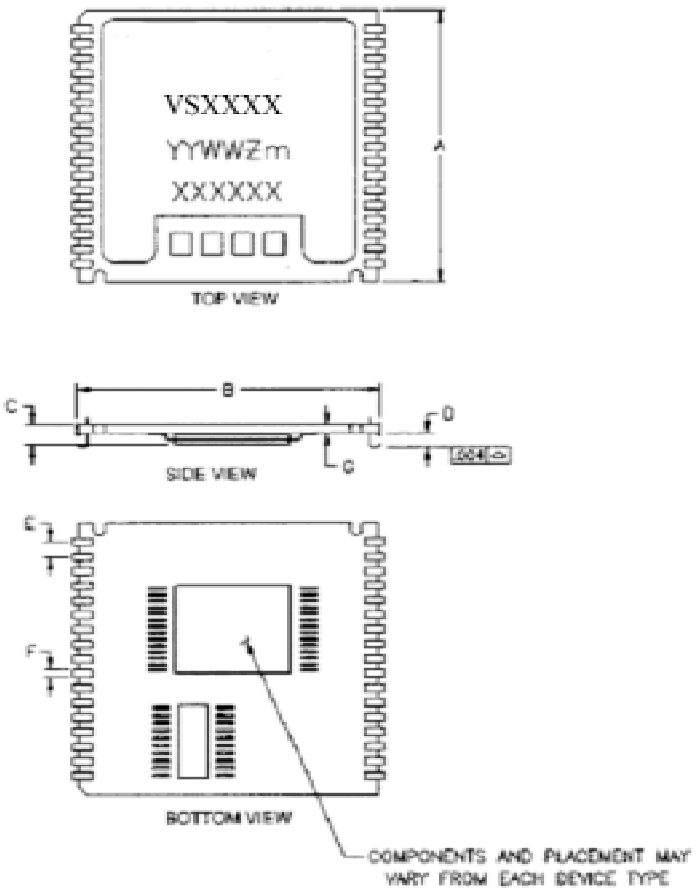
9) t_{AH2} , , t_{DH2} are measured from $\overline{CE}$ going high.

VS1744 28-PIN PACKAGE



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.470	1.490
MM	37.34	37.85
B IN.	0.675	0.740
MM	17.75	18.80
C IN.	0.335	0.355
MM	8.51	9.02
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

VS1744P



PKG	INCHES		
DIM	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.980	0.985	0.990
C	—	—	0.080
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.025	0.027	0.030

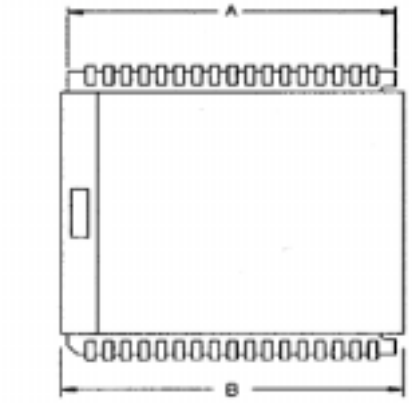
NOTE:

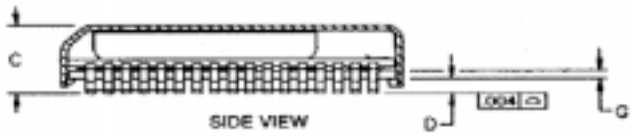
Recommends that PowerCap module bases experience one pass through solder reflow oriented with the label side up (“live – bug”).

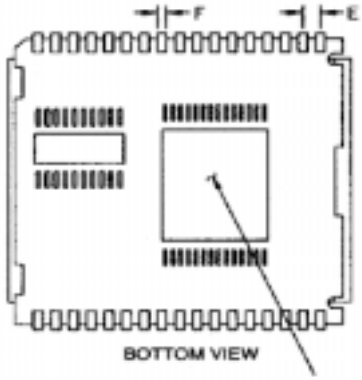
Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad, and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows, and use a solder wick to remove solder.

VS1744P WITH PowerCap ATTACHED

PKG	INCHES		
DIM	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.955	0.960	0.965
C	0.240	0.245	0.250
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030

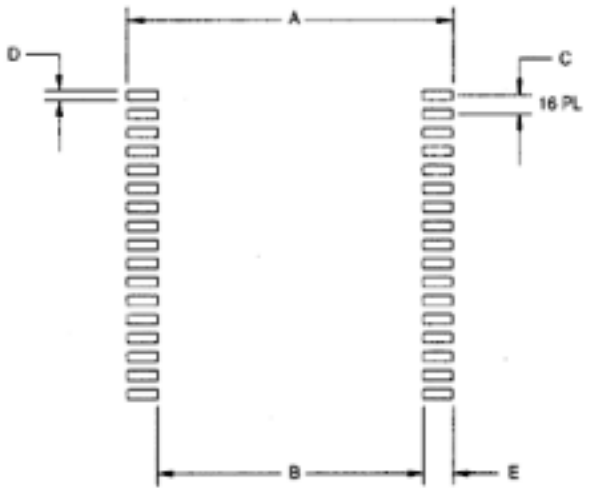






COMPONENTS AND PLACEMENT CAN VARY AMONG EACH DEVICE.

RECOMMENDED POWERCAP MODULE LAND PATTERN



PKG	INCHES		
DIM	MIN	NOM	MAX
A	—	1.050	—
B	—	0.826	—
C	—	0.050	—
D	—	0.030	—
E	—	0.112	—