# VOSSEL

**VS1747**

## Y2KC Nonvolatile Timekeeping RAM

## FEATURES

- Integrated NV SRAM, real-time clock, crystal, power-fail control circuit and lithium energy source
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Century byte register (Y2K compliant)
- Totally nonvolatile with over 10 years of operation in the absence of power
- BCD coded century, year, month, date, day, hours, minutes, and seconds with automatic leap year compensation valid up to the year 2100
- Battery voltage level indicator flag
- Power-fail write protection allows for ±10% $V_{CC}$ power supply tolerance
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- DIP Module only
  - Standard JEDEC bytewide 512k x 8 static RAM pinout
- PowerCap Module Board only
  - Surface mountable package for direct connection to PowerCap containing battery and crystal
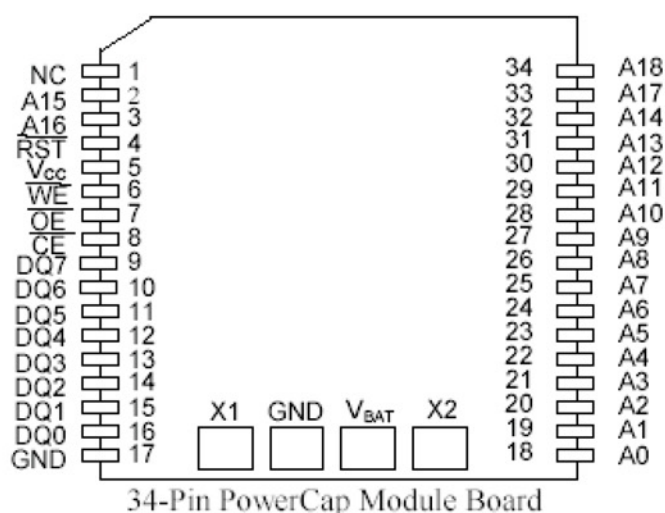  - Replaceable battery (PowerCap)

- Power-On Reset Output

## PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| A18 | 1 | 32 | $V_{CC}$ |
| A16 | 2 | 31 | A15 |
| A14 | 3 | 30 | A17 |
| A12 | 4 | 29 | $\overline{WE}$ |
| A7 | 5 | 28 | A13 |
| A6 | 6 | 27 | A8 |
| A5 | 7 | 26 | A9 |
| A4 | 8 | 25 | A11 |
| A3 | 9 | 24 | $\overline{OE}$ |
| A2 | 10 | 23 | A10 |
| A1 | 11 | 22 | $\overline{CE}$ |
| A0 | 12 | 21 | DQ7 |
| DQ0 | 13 | 20 | DQ6 |
| DQ1 | 14 | 19 | DQ5 |
| DQ2 | 15 | 18 | DQ4 |
| GND | 16 | 17 | DQ3 |

512k X 8
32-Pin Encapsulated Package

| | | | |
|---|---|---|---|
| NC | 1 | 34 | A18 |
| A15 | 2 | 33 | A17 |
| A16 | 3 | 32 | A14 |
| $\overline{RST}$ | 4 | 31 | A13 |
| $V_{CC}$ | 5 | 30 | A12 |
| $\overline{WE}$ | 6 | 29 | A11 |
| $\overline{OE}$ | 7 | 28 | A10 |
| $\overline{CE}$ | 8 | 27 | A9 |
| DQ7 | 9 | 26 | A8 |
| DQ6 | 10 | 25 | A7 |
| DQ5 | 11 | 24 | A6 |
| DQ4 | 12 | 23 | A5 |
| DQ3 | 13 | 22 | A4 |
| DQ2 | 14 | 21 | A3 |
| DQ1 | 15 | 20 | A2 |
| DQ0 | 16 | 19 | A1 |
| GND | 17 | 18 | A0 |

X1  GND  $V_{BAT}$  X2

34-Pin PowerCap Module Board

## PIN DESCRIPTION

A0–A18            – Address Input

$\overline{CE}$            – Chip Enable

$\overline{OE}$            – Output Enable

$\overline{WE}$            – Write Enable

$V_{CC}$            – Power Supply Input

GND            – Ground

DQ0–DQ7            – Data Input/Output

NC            – No Connection

$\overline{RST}$            – Power–on Reset Output(PowerCap Module board only)

X1, X2            – Crystal Connection

$V_{BAT}$            – Battery Connection

## ORDERING INFORMATION

VS1747P       (5V)

                   blank     32-pin DIP Module

                   P         34-pin PowerCap Module board*

VS1747WP      (3.3V)

                   blank     32-pin DIP Module

                   P         34-pin PowerCap Module board*

## DESCRIPTION

The VS1747 is a full function, year 2000 compliant (Y2KC), real–time clock/calendar (RTC) and 512k x 8 non–volatile static RAM. User access to all registers within the VS1747 is accomplished with a bytewide interface as shown in Figure 1. The Real-time clock (RTC) information and control bits reside in the eight upper most RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the date of each month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data.

The VS1747 also contains its own power–fail circuitry which deselects the device when the $V_{CC}$ supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low $V_{CC}$ as errant access and update cycles are avoided.

## VS1747 BLOCK DIAGRAM Figure 1
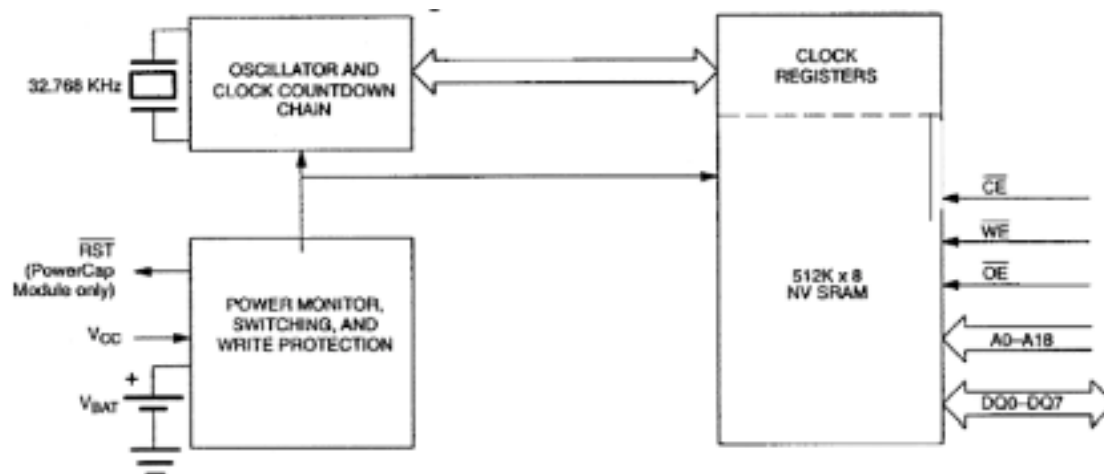


## PACKAGES

The VS1747 is available in two packages (32–pin DIP and 34–pin PowerCap module). The 32–pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34–pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap that contains the crystal and battery. This design allows the Power-Cap to be mounted on top of the VS1747P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers.

## CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the VS1747 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a one is written into the read bit, bit 6 of the century register, see Table 2. As long as a one remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the VS1747 registers are updated simultaneously after the internal clock register updating process has been re–enabled. Updating is within a second after the read bit is written to zero. The READ bit must be set to a zero for a minimum of 500µs to ensure the external registers will be updated.

## VS1747 TRUTH TABLE Table 1

| V$_{CC}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|
| | V$_{IH}$ | X | X | DESELECT | HIGH-Z | STANDBY |
| V$_{CC}$>V$_{PF}$ | V$_{IL}$ | X | V$_{IL}$ | WRITE | DATA IN | ACTIVE |
| | V$_{IL}$ | V$_{IL}$ | V$_{IH}$ | READ | DATA OUT | ACTIVE |
| | V$_{IL}$ | V$_{IH}$ | V$_{IH}$ | READ | HIGH-Z | ACTIVE |
| V$_{SO}$<V$_{CC}$<V$_{PF}$ | X | X | X | DESELECT | HIGH-Z | CMOS STANDBY |
| V$_{CC}$<V$_{SO}$<V$_{PF}$ | X | X | X | DESELECT | HIGH-Z | DATA RETENTION MODE |

## SETTING THE CLOCK

As shown in Table 2, bit 7 of the century register is the write bit. Setting the write bit to a one, like the read bit, halts updates to the VS1747 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a zero then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB (bit 7) of the seconds registers, see Table 2. Setting it to a one stops the oscillator.

## FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, $\overline{WE}$ high, and address for seconds register remain valid and stable).

## CLOCK ACCURACY (DIP MODULE)

The VS1747 is guaranteed to keep time accuracy to within ± 1 minute per month at 25℃. The RTC is calibrated at the factory using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also effected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information
please see application note 58.

## CLOCK ACCURACY (POWERCAP MODULE)

The VS1747 individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ± 1.53 minutes per month (35 ppm) at 25°C. Clock accuracy is also effected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information please see application note 58.

## VS1746 REGISTER MAP Table 2

| ADDRESS | DATA | | | | | | | | FUNCTION/RANGE | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 7FFFF | 10 YEAR | | | | YEAR | | | | YEAR | 00-99 |
| 7FFFE | X | X | X | 10 MO | MONTH | | | | MONTH | 01-12 |
| 7FFFD | X | X | 10 DATE | | DATE | | | | DATE | 01-31 |
| 7FFFC | BF | FT | X | X | X | DAY | | | DAY | 01-07 |
| 7FFFB | X | X | 10 HOUR | | HOUR | | | | HOUR | 00-23 |
| 7FFFA | X | 10 MINUTES | | | MINUTES | | | | MINUTES | 00-59 |
| 7FFF9 | $\overline{OSC}$ | 10 SECONDS | | | SECONDS | | | | SECONDS | 00-59 |
| 7FFF8 | W | R | 10 CENTURY | | CENTURY | | | | CENTURY | 00-39 |

$\overline{OSC}$ = STOP BIT          R = READ BIT          FT = FREQUENCY TEST
W = WRITE BIT          X = SEE NOTE BELOW          BF = BATTERY FLAG

## NOTE:

All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

## RETRIEVING DATA FROM RAM OR CLOCK

The VS1747 is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within $t_{AA}$ after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times and states are not met, valid data will be available at the latter of chip enable access ($t_{CEA}$) or at output enable access time ($t_{OEA}$) . The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$ . If the outputs are activated before $t_{AA}$, the data lines are driven to an intermediate state until $t_{AA}$. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time ($t_{OH}$ ) but will then go indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The VS1747 is in the write mode whenever $\overline{WE}$, and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of $t_{WR}$ prior to the initiation of another read or write cycle. Data in must be valid $t_{DS}$ prior to the end of write and remain valid for $t_{DH}$ afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the output $t_{WEZ}$ after $\overline{WE}$ goes active.

## DATA RETENTION MODE

The 5-volt device is fully accessible and data can be written or read only when $V_{CC}$ is greater than $V_{PF}$. However, when $V_{CC}$ is below the power failing point, $V_{PF}$, (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access. At this time the power fail reset output signal ($\overline{RST}$) is driven active and will remain active until $V_{CC}$ returns to nominal levels. When $V_{CC}$ falls below the battery switch point $V_{SO}$ (battery supply level), device power is switched from the $V_{CC}$ pin to the backup battery. RTC operation and SRAM data are maintained from the battery until $V_{CC}$ is returned to nominal levels. The 3.3 volt device is fully accessible and data can be written or read only when $V_{CC}$ is greater than $V_{PF}$. When $V_{CC}$ falls below the power fail point, $V_{PF}$, access to the device is inhibited. At this time the power fail reset output signal ($\overline{RST}$) is driven active and will remain active until $V_{CC}$ returns to nominal levels. If $V_{PF}$ is less than $V_{SO}$, the device power is switched from $V_{CC}$ to the backup supply ($V_{BAT}$) when $V_{CC}$ drops below $V_{PF}$. If VPF is greater than Vso, the device power is switched from $V_{CC}$ to the backup supply ($V_{BAT}$) when $V_{CC}$ drops below Vso. RTC operation and SRAM data are maintained from the battery until $V_{CC}$ is returned to nominal levels. The $\overline{RST}$ signal is an open drain output and requires a pull up. Except for the $\overline{RST}$, all control, data, and address signals must be powered down when $V_{CC}$ is powered down.

## BATTERY LONGEVITY

The VS1747 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the $V_{CC}$ supply is not present. The capability of this internal power supply is sufficient to power the VS1747 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25℃ with the internal clock oscillator running in the absence of $V_{CC}$ power. Each VS1747 is shipped with its lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is first applied at a level greater than $V_{PF}$ , the lithium energy source is enabled for battery backup operation. Actual life expectancy of the VS1747 will be much longer than 10 years since no lithium battery energy is consumed when $V_{CC}$ is present.

## BATTERY MONITOR

The VS1747 constantly monitors the battery voltage of the internal battery. The Battery Flag bit (bit 7) of the day register is used to indicate the voltage level range of the battery. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC and RAM are questionable.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | –0.3V to +6.0V |
| Storage Temperature | –40℃ to +85℃ |
| Soldering Temperature | 260°C for 10 seconds (DIP Package) (See Note 7) |
| | See IPC/JEDEC Standard J-STD-020A for |
| | Surface Mount Devices |

## OPERATING RANGE

| Range | Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 10% or 5V ± 10% |

## RECOMMENDED DC OPERATING CONDITIONS

(Over the Operating Range)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 Voltage All Inputs $V_{CC}$ = 5V±10% | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 V | V | 1 |
| $V_{CC}$ = 3.3V±10% | $V_{IH}$ | 2.0 | | $V_{CC}$+0.3 V | V | 1 |
| Logic 0 Voltage All Inputs $V_{CC}$ = 5V±10% | $V_{IL}$ | -0.3 | | 0.8 | V | 1 |
| $V_{CC}$ = 3.3V±10% | $V_{IL}$ | -0.3 | | 0.6 | V | 1 |

# DC ELECTRICAL CHARACTERISTICS

(Over the Operating Range; $V_{CC}$ = 5.0V $\pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Active Supply Current | $I_{CC}$ | | | 85 | mA | 2,3 |
| TTL Standby Current ($\overline{CE}$ = $V_{IH}$) | $I_{CC1}$ | | | 6 | mA | 2,3 |
| CMOS Standby Current ($\overline{CE}$ $\geq V_{CC}$-0.2V) | $I_{CC2}$ | | | 4 | mA | 2,3 |
| Input Leakage Current (any input) | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current (any output) | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = -1.0 mA) | $V_{OH}$ | 2.4 | | | | 1 |
| Output Logic 0 Voltage ($I_{OUT}$ = +2.1 mA) | $V_{OL}$ | | | 0.4 | | 1 |
| Write Protection Voltage | $V_{PF}$ | 4.25 | | 4.50 | V | 1 |
| Battery Switch Over Voltage | $V_{SO}$ | | $V_{BAT}$ | | | 1,4 |

# DC ELECTRICAL CHARACTERISTICS

(Over the Operating Range; $V_{CC}$ = 3.3V $\pm$ 10%)

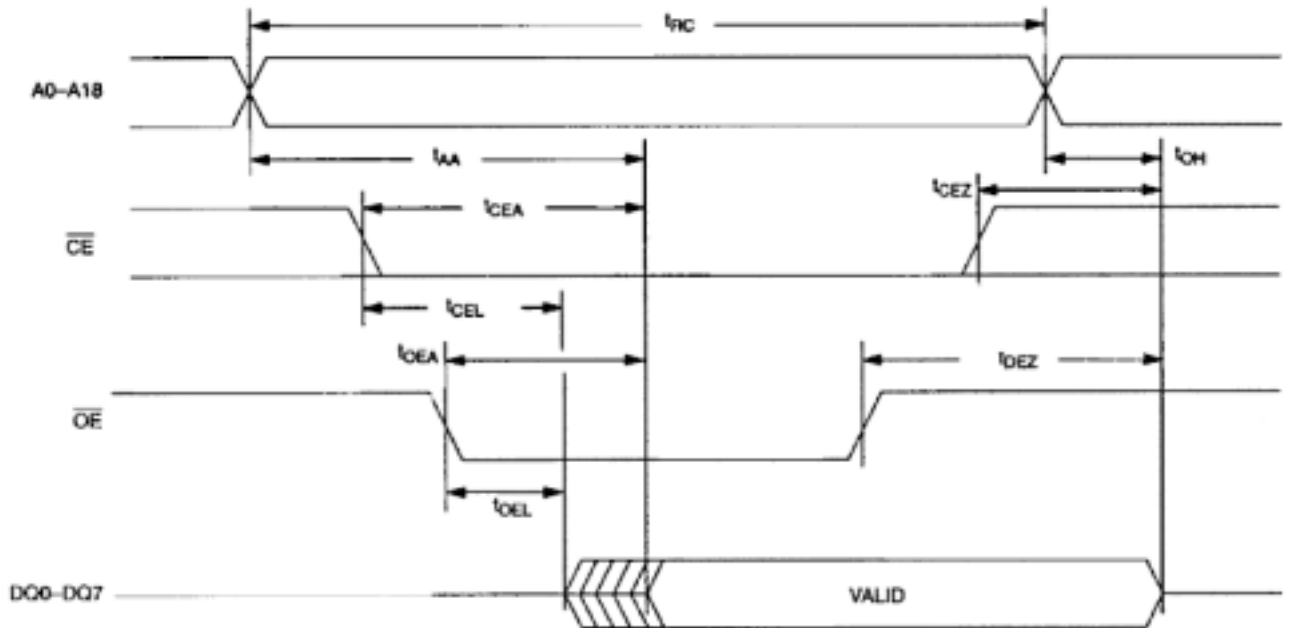| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Active Supply Current | $I_{CC}$ | | | 30 | mA | 2,3 |
| TTL Standby Current ($\overline{CE}$ = $V_{IH}$) | $I_{CC1}$ | | | 2 | mA | 2,3 |
| CMOS Standby Current ($\overline{CE}$ $\geq V_{CC}$-0.2V) | $I_{CC2}$ | | | 2 | mA | 2,3 |
| Input Leakage Current (any input) | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current (any output) | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = -1.0 mA) | $V_{OH}$ | 2.4 | | | | 1 |
| Output Logic 0 Voltage ($I_{OUT}$ = +2.1 mA) | $V_{OL}$ | | | 0.4 | | 1 |
| Write Protection Voltage | $V_{PF}$ | 2.80 | | 2.97 | V | 1 |
| Battery Switch Over Voltage | $V_{SO}$ | | $V_{BAT}$ or $V_{PF}$ | | V | 1,4 |

## READ CYCLE, AC CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 70 | | | ns | |
| Address Access Time | $t_{AA}$ | | | 70 | ns | |
| $\overline{CE}$ to DQ Low-Z | $t_{CEL}$ | 5 | | | ns | |
| $\overline{CE}$ E Access Time | $t_{CEA}$ | | | 70 | ns | |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | | 25 | ns | |
| $\overline{OE}$ to DQ Low-Z | $t_{OEL}$ | 5 | | | ns | |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | | 35 | ns | |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | | 25 | ns | |
| Output Hold from Address | $t_{OH}$ | 5 | | | ns | |

## READ CYCLE, AC CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 3.3V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 120 | | | ns | |
| Address Access Time | $t_{AA}$ | | | 120 | ns | |
| $\overline{CE}$ to DQ Low-Z | $t_{CEL}$ | 5 | | | ns | |
| $\overline{CE}$ E Access Time | $t_{CEA}$ | | | 120 | ns | |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | | 40 | ns | |
| $\overline{OE}$ to DQ Low-Z | $t_{OEL}$ | 5 | | | ns | |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | | 100 | ns | |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | | 35 | ns | |
| Output Hold from Address | $t_{OH}$ | 5 | | | ns | |

## READ CYCLE TIMING DIAGRAM



## WRITE CYCLE, AC CHARACTERISTICS

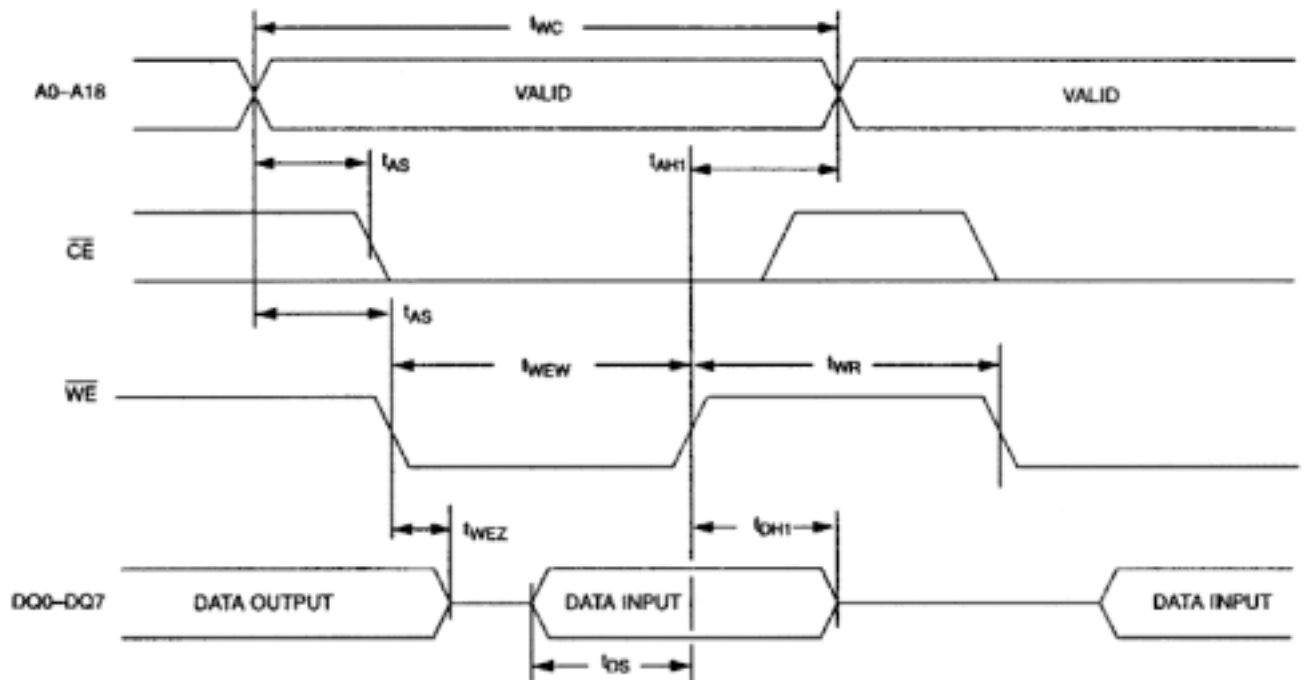(Over the Operating Range; $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 70 | | | ns | |
| Address Setup Time | $t_{AS}$ | 0 | | | ns | |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 50 | | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 60 | | | ns | |
| Data Setup Time | $t_{DS}$ | 30 | | | ns | |
| Data Hold Time | $t_{DH1}$ | 0 | | | ns | 8 |
| Data Hold Time | $t_{DH2}$ | 0 | | | ns | 9 |
| Address Hold Time | $t_{AH1}$ | 5 | | | ns | 8 |
| Address Hold Time | $t_{AH2}$ | 5 | | | ns | 9 |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | | 25 | ns | |
| Write Recovery Time | $t_{WR}$ | 5 | | | ns | |

## WRITE CYCLE, AC CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 3.3V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 120 | | | ns | |
| Address Setup Time | $t_{AS}$ | 0 | | 120 | ns | |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 100 | | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 110 | | | ns | |
| $\overline{CE}$ and CE2 Pulse Width | $t_{CEW}$ | 110 | | | ns | |
| Data Setup Time | $t_{DS}$ | 80 | | | ns | |
| Data Hold Time | $t_{DH1}$ | 0 | | | ns | 8 |
| Data Hold Time | $t_{DH2}$ | 0 | | | ns | 9 |
| Address Hold Time | $t_{AH1}$ | 0 | | | ns | 8 |
| Address Hold Time | $t_{AH2}$ | 10 | | | ns | 9 |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | | 40 | ns | |
| Write Recovery Time | $t_{WR}$ | 10 | | | ns | |

## WRITE CYCLE TIMING DIAGRAM, WRITE ENABLE CONTROLLED

## WRITE CYCLE TIMING DIAGRAM, CHIP ENABLE CONTROLLED
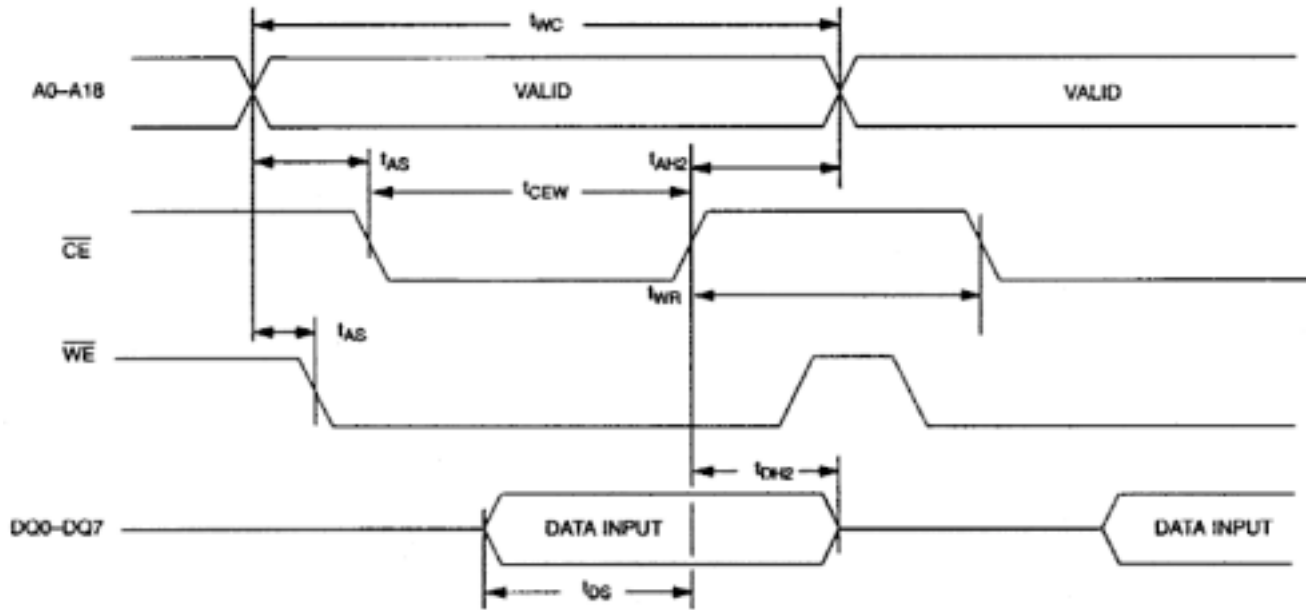


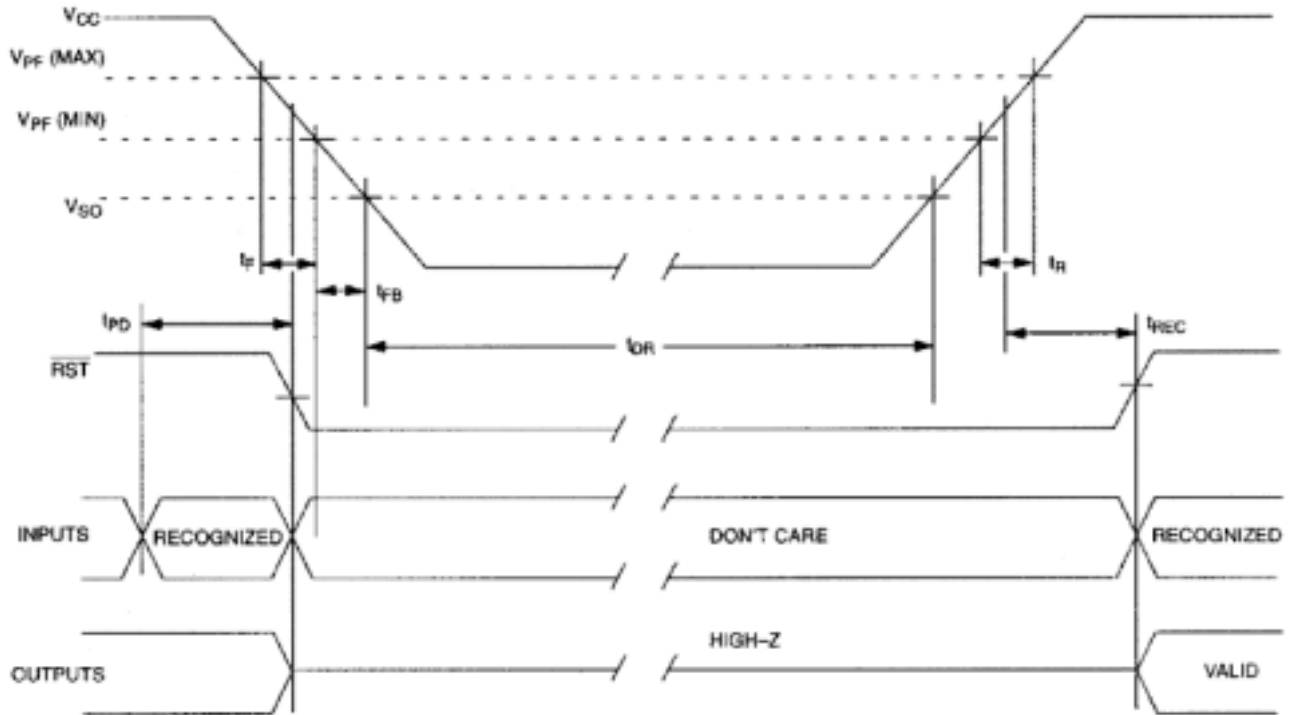## POWER–UP/DOWN AC CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 5.0V \pm 10\%$)

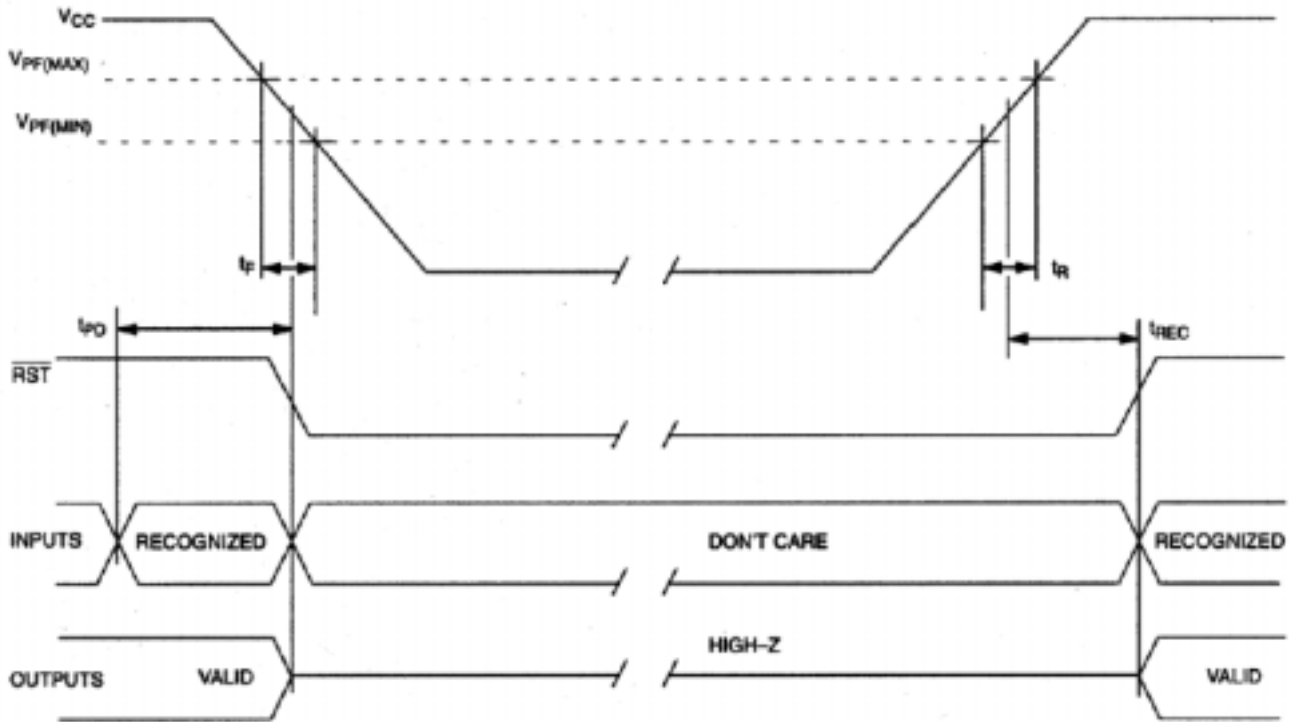| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_H$ Before Power-down | $t_{PD}$ | 0 | | | μs | |
| $V_{CC}$ Fall Time: $V_{PF}$(MAX) to $V_{PF}$(MIN) | $t_F$ | 300 | | | μs | |
| $V_{CC}$ Fall Time: $V_{PF}$(MIN) to $V_{SO}$ | $t_{FB}$ | 10 | | | μs | |
| $V_{CC}$ Rise Time: $V_{PF}$(MIN) to $V_{PF}$(MAX) | $t_R$ | 0 | | | μs | |
| Power-up Recover Time | $t_{REC}$ | | | 35 | ms | |
| Expected Data Retention Time (Oscillator ON) | $t_{DR}$ | 10 | | | years | 5,6 |

## POWER−UP/POWER−DOWN TIMING 5 VOLT DEVICE



## POWER−UP/DOWN CHARACTERISTICS

(Over the Operating Range; $V_{CC} = 3.3V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_H$, Before Power-down | $t_{PD}$ | 0 | | | μs | |
| $V_{CC}$ Fall Time: $V_{PF}$(MAX) to $V_{PF}$(MIN) | $t_F$ | 300 | | | μs | |
| $V_{CC}$ Rise Time: $V_{PF}$(MIN) to $V_{PF}$(MAX) | $t_R$ | 0 | | | μs | |
| $V_{PF}$ to $\overline{RST}$ High | $t_{REC}$ | | | 35 | ms | |
| Expected Data Retention Time (Oscillator ON) | $t_{DR}$ | 10 | | | years | 5,6 |

## POWER−UP/DOWN WAVEFORM TIMING 3.3 VOLT DEVICE



## CAPACITANCE                                    ($t_A = 25℃$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Capacitance on all input pins | $C_{IN}$ | | | 7 | pF | |
| Capacitance on all output pins | $C_O$ | | | 10 | pF | |

## AC TEST CONDITIONS

Output Load:            100 pF + 1TTL Gate
Input Pulse Levels:     0.0 to 3.0V

Timing Measurement Reference Levels:
     Input: 1.5V
     Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

## NOTES:

1. Voltages are referenced to ground.
2. Typical values are at $25℃$ and nominal supplies.

3. Outputs are open.

4. Battery switch over occurs at the lower of either the battery terminal voltage or $V_{PF}$.

5. Data retention time is at 25℃.

6. Each VS1747 has a built–in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined for DIP modules and assembled PowerCap modules as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.

7. Real–Time Clock Modules (DIP) can be successfully processed through conventional wave–soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85℃. Post solder cleaning with water washing techniques is acceptable, provided that ultra-sonic vibration is not used.

In addition, for the PowerCap:
   a. recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up ("live – bug").
   b. Hand Soldering and touch–up: Do not touch or apply the soldering iron to leads for more than 3 (three) seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.

8. $t_{AH1}$, $t_{DH1}$ are measured from $\overline{WE}$ going high.

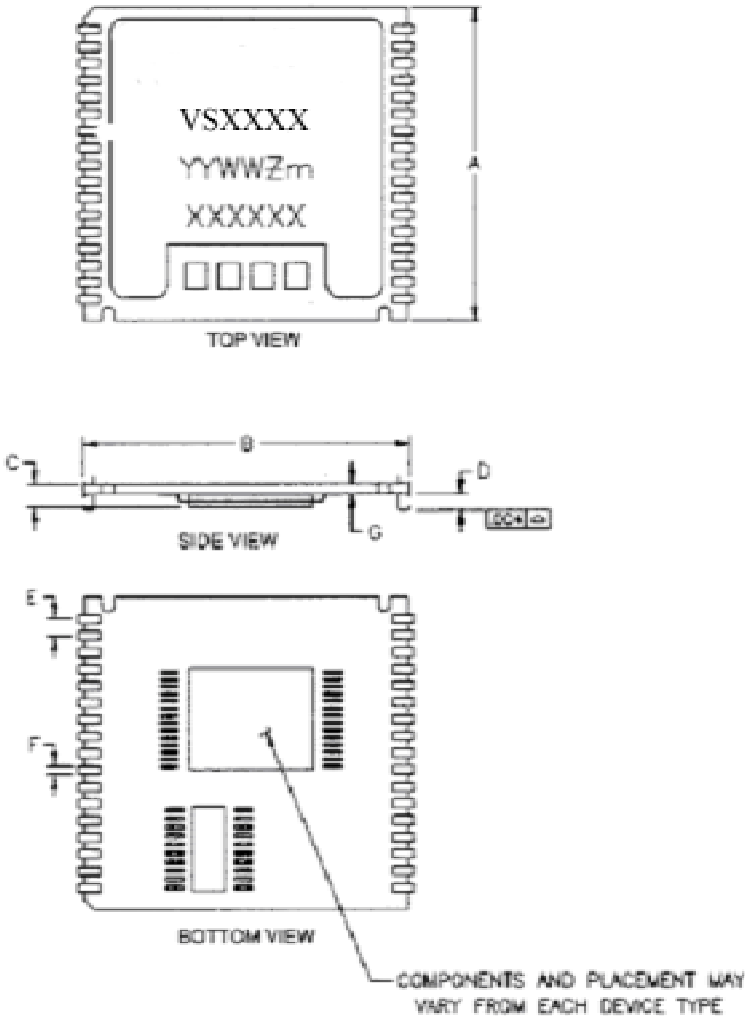9. $t_{AH2}$, $t_{DH2}$ are measured from $\overline{CE}$ going high.

## VS1747 32-PIN PACKAGE
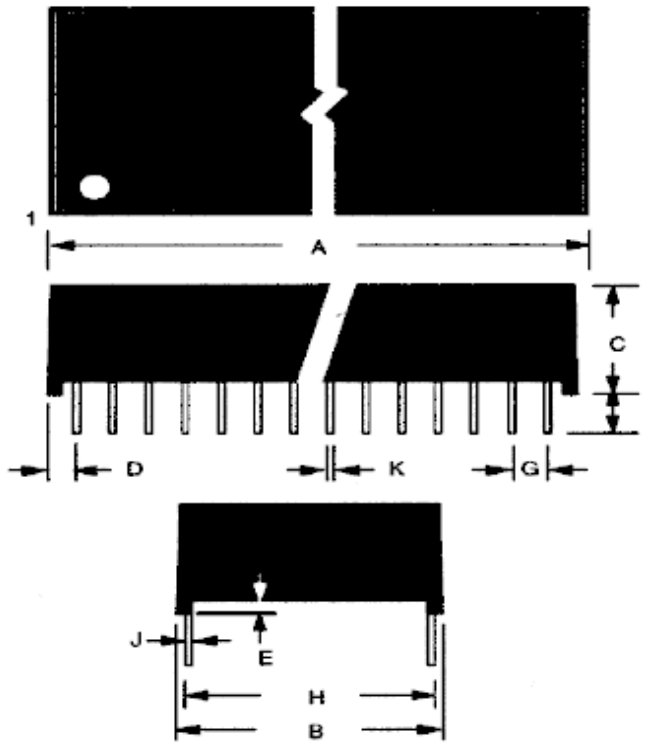


| PKG | 32-PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A    IN. | 1.680 | 1.740 |
| MM | 42.67 | 44.20 |
| B    IN. | 0.715 | 0.740 |
| MM | 18.16 | 18.80 |
| C    IN. | 0.335 | 0.365 |
| MM | 8.51 | 9.27 |
| D    IN. | 0.075 | 0.105 |
| MM | 1.91 | 2.67 |
| E    IN. | 0.015 | 0.030 |
| MM | 0.38 | 0.76 |
| F    IN. | 0.140 | 0.180 |
| MM | 3.56 | 4.57 |
| G    IN. | 0.090 | 0.110 |
| MM | 2.29 | 2.79 |
| H    IN. | 0.590 | 0.630 |
| MM | 14.99 | 16.00 |
| J    IN. | 0.010 | 0.018 |
| MM | 0.25 | 0.46 |
| K    IN. | 0.015 | 0.025 |
| MM | 0.38 | 0.64 |

## VS1747P

| PKG | INCHES | | |
|-----|--------|--------|--------|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.980 | 0.985 | 0.990 |
| C | - | - | 0.080 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.025 | 0.027 | 0.030 |

VSXXXX
YYWWZm
XXXXXX

TOP VIEW

SIDE VIEW

BOTTOM VIEW

COMPONENTS AND PLACEMENT MAY
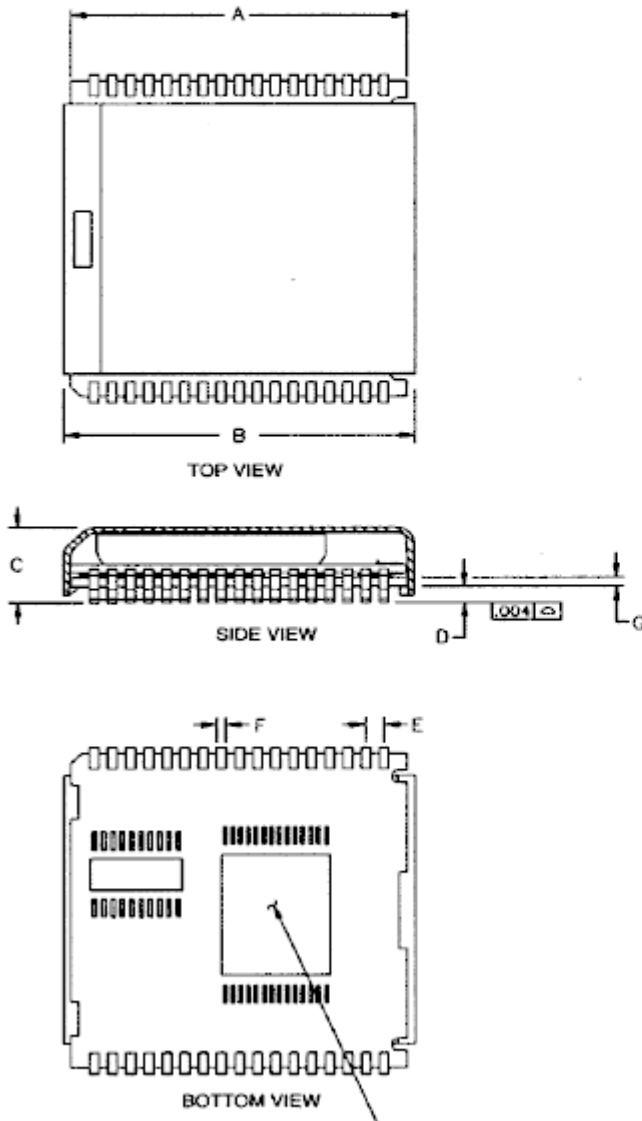VARY FROM EACH DEVICE TYPE

## NOTE:

recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up ("live – bug").

Hand Soldering and touch–up: Do not touch or apply the soldering iron to leads for more than 3 (three) seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To

remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.

## VS1747P WITH PowerCap ATTACHED

| PKG | INCHES | | |
|-----|-----|-----|-----|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.955 | 0.960 | 0.965 |
| C | 0.240 | 0.245 | 0.250 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.020 | 0.025 | 0.030 |

TOP VIEW

SIDE VIEW

BOTTOM VIEW

COMPONENTS AND PLACEMENT MAY
VARY FROM EACH DEVICE TYPE

## RECOMMENDED POWERCAP MODULE LAND PATTERN

| PKG DIM | INCHES | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 1.050 | - |
| B | - | 0.826 | - |
| C | - | 0.050 | - |
| D | - | 0.030 | - |
| E | - | 0.112 | - |